# PAC5232 Data Sheet

***Power Application Controller®***

Multi-Mode Power Manager™

Configurable Analog Front End™

Application Specific Power Drivers™

ARM© Cortex®-M0 Controller Core



Rev 1.1
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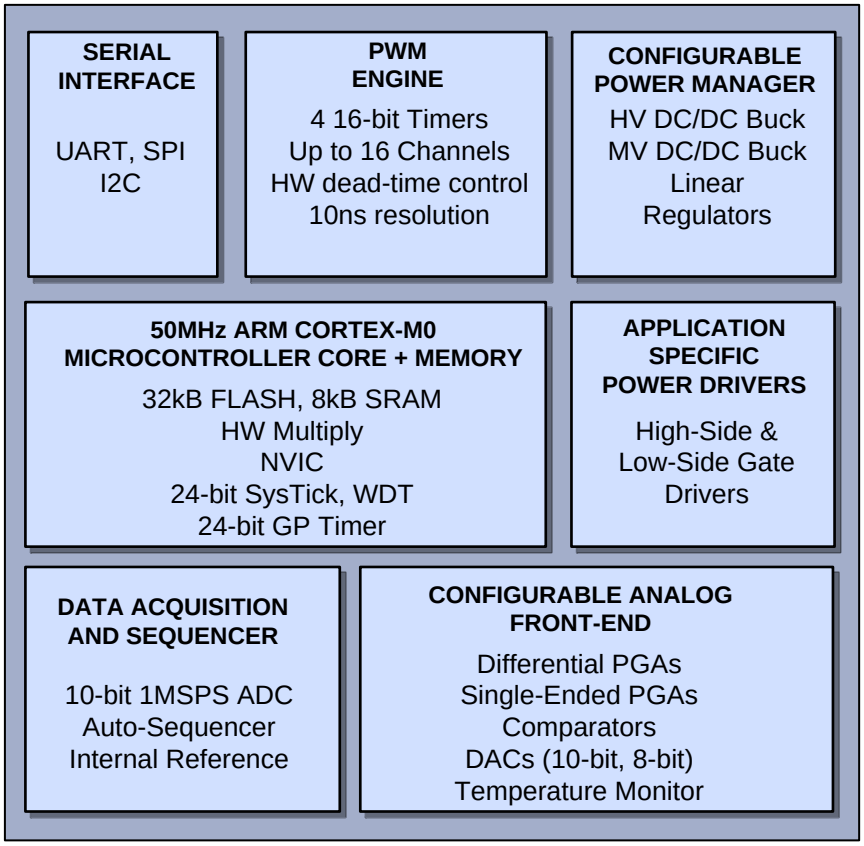
# 1 GENERAL DESCRIPTION

The PAC5232 is a Power Application Controller® (PAC) product that is optimized for high-speed motor control and driving. The PAC5232 integrates a 50MHz ARM Cortex®-M0 32-bit microcontroller core with a highly-configurable Power manager, Active-Semi's proprietary and patent-pending Configurable Analog Front-End™ and Application Specific Power Drivers™ to form the most compact microcontroller-based power and motor control solution available.

The PAC5232 microcontroller features 32kB of embedded FLASH and 8kB of SRAM memory, a 1MSPS analog-to-digital converter (ADC) with programmable auto-sequencer, 3.3V/5V IO, flexible clock control system, PWM and general-purpose timers and several serial communications interfaces.

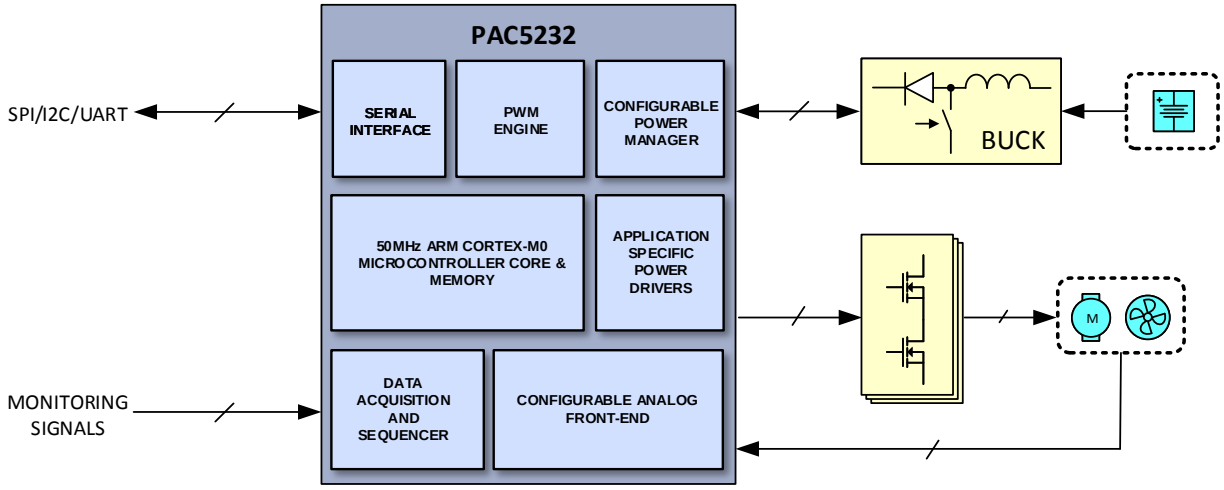
The Configurable Power Manager (CPM) provides "all-in-one" efficient power management solution for multiple types of power sources. It features a configurable high-voltage switching supply controller capable of operating a buck converter, a configurable medium-voltage switching regulator, and four linear regulated voltage supplies. The Application Specific Power Drivers (ASPD) are 180V power drivers designed for half bridge, H-bridge, 3-phase, and general purpose driving. The Configurable Analog Front End (CAFE) comprises differential programmable gain amplifiers, single-ended programmable gain amplifiers, comparators, digital-to-analog converters, and I/Os for programmable and inter-connectible signal sampling, feedback amplification, and sensor monitoring of multiple analog input signals.




The PAC5232 is available in a 51-pin, 8x8mm TQFN package.

# 2 PAC® FAMILY APPLICATIONS

- Garden Tools
- Telecom Fans
- Light Electric Vehicle
- Battery Powered Motor Controllers and Drivers from 48VC – 120VDC



# 3 PRODUCT SELECTION SUMMARY

| PART NUMBER | PIN PKG | POWER MANAGER | | CONFIGURABLE ANALOG FRONT END | | | | | APPLICATION SPECIFIC POWER DRIVERS | | | MCU | | | | | APPLICATION |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | INPUT VOLTAGE | DC/DC | DIFF-PGA | PGA | COMPARATOR | DAC | ADC CHANNEL | VBST/VSRC | POWER DRIVER | PWM CHANNEL | SPEED (MHz) | FLASH (kB) | SRAM (kB) | GPIO | SERIAL COMM | |
| **PAC5232** | 51L 8x8 QFN | 25V-160V | Y | 3 | 4 | 10 | 2 | 9 | 180V | 3 LS (2A) 3 HS (2A) | 6@VP 6@VCCIO | 50 | 32 | 8 | 29 | UART SPI I2C SWD | 3 half-bridge 3 phase control<br><br>BEMF Trapezoidal or FOC |

Notes: DIFF-PGA = differential programmable gain amplifier; HS = high-side, LS = low-side, PGA = programmable gain amplifier, VSRC = Bootstrap Voltage Source

# 4 ORDERING INFORMATION

| PART NUMBER | TEMPERATURE RANGE | PACKAGE | PINS | PACKING |
|---|---|---|---|---|
| **PAC5232QX** | -40°C to 105°C | 51L 8x8 QFN | 51 + Exposed Pad | Tray |

# 5 FEATURES

## 5.1 Feature Overview

- **Configurable Power Manager**
  - High-voltage buck switching supply controller
    - Input Voltage: 25V – 160V
    - Configurable Output Voltage: 12V or 15V
  - 5V medium-voltage switching supply regulator
  - 3 Linear regulators with power and hibernate management
  - Power and temperature monitor, warning, fault detection
- **Proprietary Configurable Analog Front-End**
  - 10 Analog Front-End IO pins
  - 3 Differential Programmable Gain Amplifiers
  - 4 Single-ended Programmable Gain Amplifiers
  - Programmable Over-Current Protection
  - 10 Comparators
  - 2 10-bit DACs
- **Proprietary Application Specific Power Drivers**
  - 3 180V high-side gate drivers with 2A gate driving capability
  - 3 low-side gate drivers with 2A gate driving capability
  - Configurable propagation delay and fault protection
- **3.3V I/Os**
  - 2 general-purpose I/Os with tri-state and dedicated analog input to ADC
- **True 5V I/Os**
  - 11 general-purpose I/Os with tri-state, pull-up, pull-down and dedicated I/O supply
  - Configurable as true 5V or 3.3V I/Os
- **50MHz ARM© Cortex®-M0 32-bit Microcontroller Core**
  - Single-cycle 32-bit x 32-bit hardware multiplier
  - Integrated sleep and deep sleep modes
  - Nested Vectored Interrupt Controller (NVIC) with 20 Interrupts with 3 levels of priority
  - 24-Bit SysTick Timer
  - Wake-up Interrupt Controller (WIC) allowing power-saving sleep modes
  - Clock-gating allowing low-power operation
- **Memory**
  - 32kB FLASH
  - 8kB SRAM
- **Analog to Digital Converter (ADC)**
  - 10-bit resolution
  - 1MSPS
  - Dual Programmable ADC Auto-Sequencers
- **Flexible clock and PLL from internal 1.25% oscillator, ring oscillator, external clock or crystal**
- **9 Timing Generators**
  - Four 16-bit timers with up to 16 PWM/CC blocks and 7 independent dead-time controllers
  - 24-bit watchdog timer
  - 4s or 8s watchdog timer
  - 24-bit real time clock
  - 24-bit SysTick timer
  - Wake-up timer for sleep modes from 0.125s to 8s
- **SPI, I2C, and UART serial communication interfaces**
- **SWD debug interface with interface disable function**

# 6 ABSOLUTE MAXIMUM RATINGS

The table below shows the absolute maximum ratings for this device.

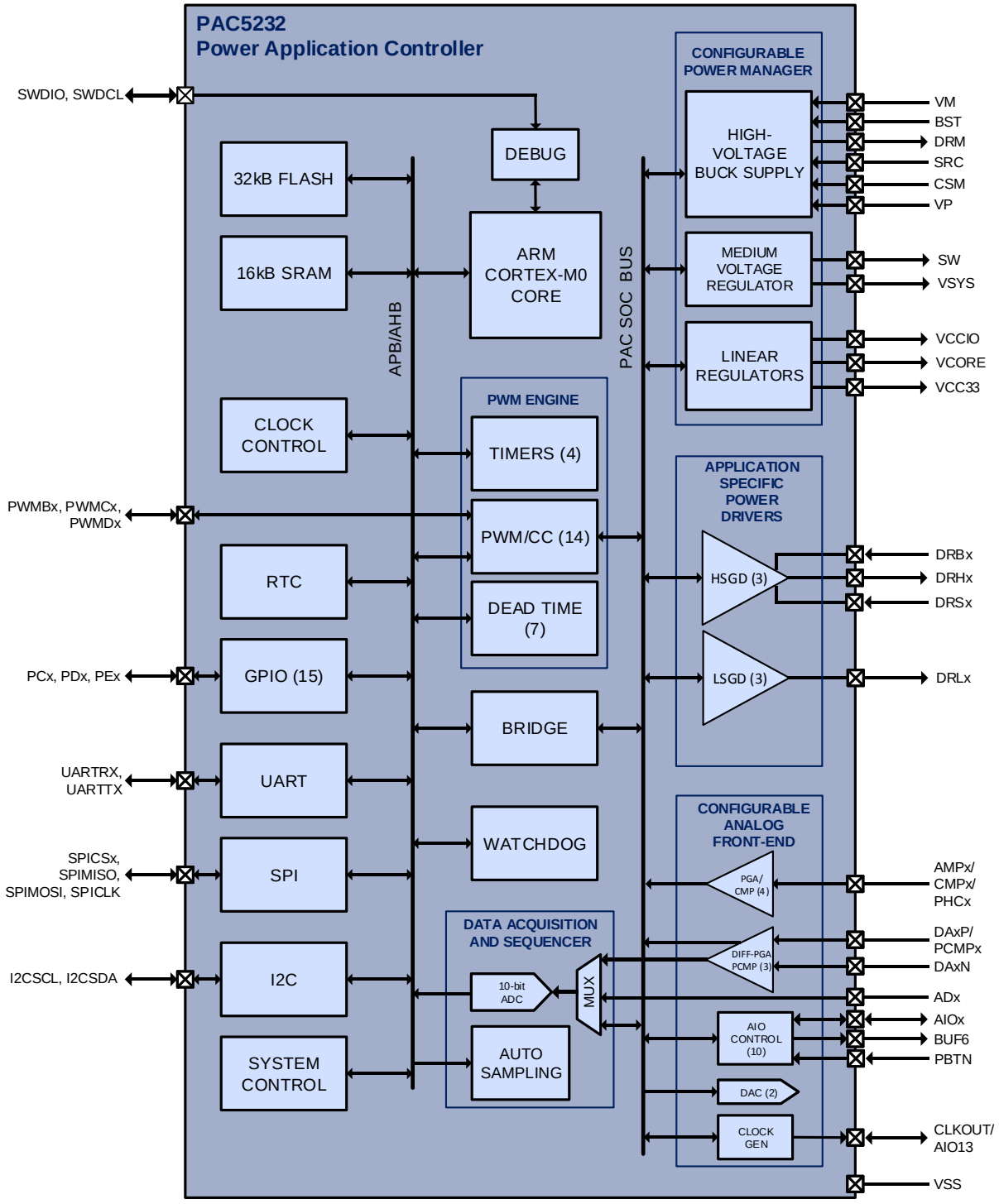
To prevent damage to the device, do not exceed these limits. Exposure to the absolute maximum rating conditions for long periods of time may affect device reliability.

The device is not guaranteed to function properly outside of the operating conditions.

| PARAMETER | | VALUE | UNIT |
|---|---|---|---|
| VM to VSS | | -0.3 to 160 | V |
| BST to VSS | | -0.3 to 180 | V |
| BST to SRC | | -0.3 to 20 | V |
| SRC to VSS | | -10 to VM + 15 | V |
| DRM to SRC | | -0.3 to BST + 0.3 | V |
| VP to VSS | | -0.3 to 20 | V |
| SW to VSS | | -0.3 to $V_P$ + 0.3 | V |
| CSM to VP | | -0.3 to 0.3 | V |
| VSYS to VSS | | -0.3 to 6 | V |
| AIO<9:7>, AIO<5:0>, VCCIO, AIO6 to VSS | | -0.3 to $V_{SYS}$ + 0.3 | V |
| PD<x>, PE<x> to VSS | | -0.3 to $V_{CCIO}$ + 0.3 | V |
| PC<x> to VSS | | -0.3 to $V_{CC33}$ + 0.3 | V |
| VCC33 to VSS | | -0.3 to 4.1 | V |
| VCORE to VSS | | -0.3 to 2.5 | V |
| DRL0, DRL1, DRL2 to VSS | | -0.3 to $V_P$ + 0.3 | V |
| DRB3, DRB4, DRB5 to VSS | | -0.3 to 180 | V |
| DRS3, DRS4, DRS5 to VSS | | -10 to VM + 15 | V |
| DRB3 to DRS3, DRB4 to DRS4, DRB5 to DRS5 | | -0.3 to 20 | V |
| DRH3 to DRS3, DRH4 to DRS4, DRH5 to DRS5 | | -0.3 to $V_{DRBx}$ + 0.3 | V |
| VSS RMS Current[1] | | 0.2 | $A_{RMS}$ |
| Operating temperature range | | -40 to 105 | °C |
| Electrostatic Discharge (ESD) | Human body model (JEDEC) | 2 | kV |
| | Charge device model (JEDEC) | 1 | kV |

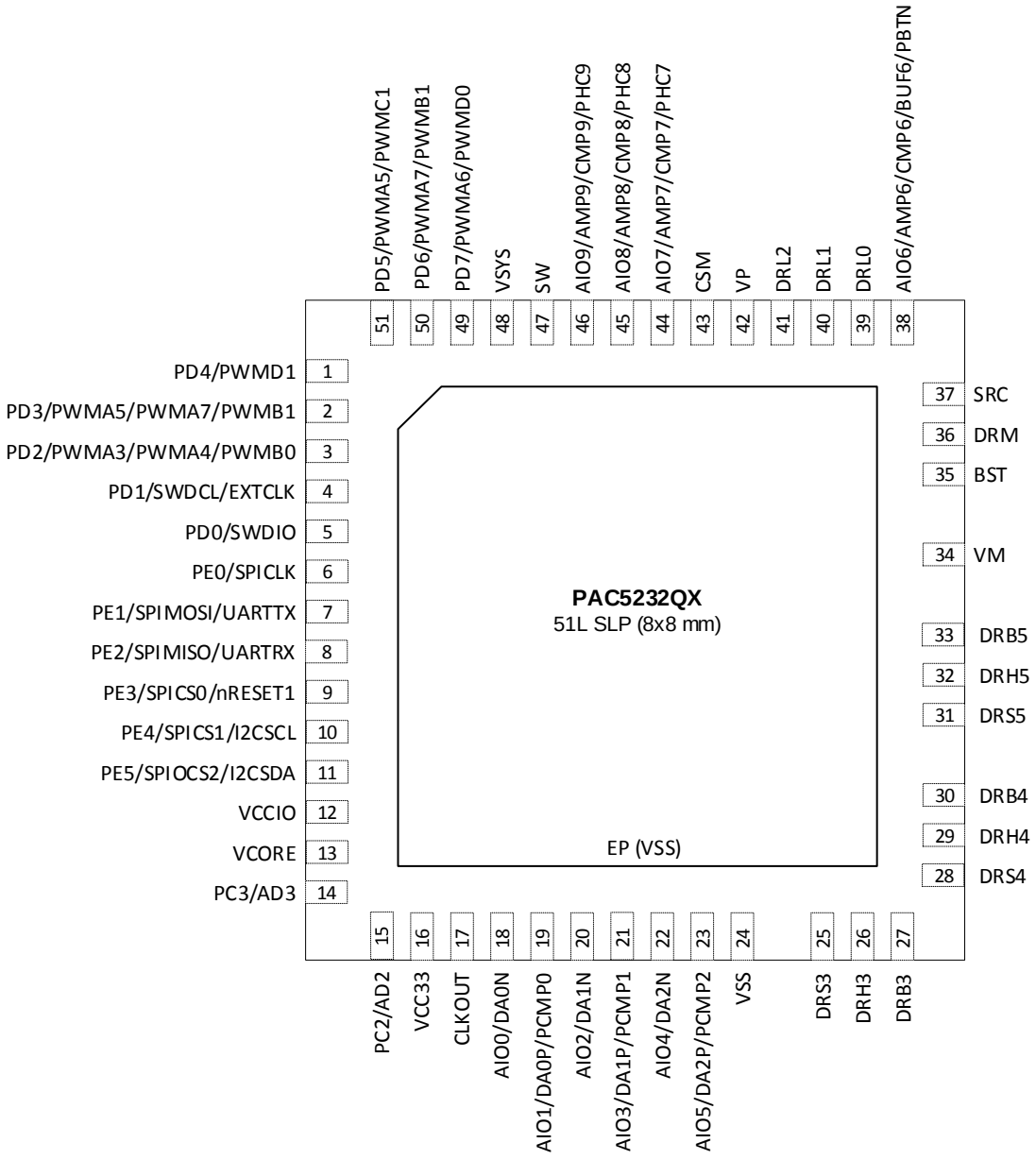
[1] Peak current may be 10 times higher than the RMS value for pulses shorter than 10µs.

# 7 ARCHITECTURAL BLOCK DIAGRAM



# 8 PIN CONFIGURATION

## 8.1 PAC5232QX Pin Configuration (51L SLP 8x8 mm Package)



# 9 PIN DESCRIPTION

## 9.1 Power and Ground Pin Description

| PIN NAME | PIN NUMBER | TYPE | DESCRIPTION |
|---|---|---|---|
| VCCIO | 12 | Power | Internally generated digital I/O 3.3V power supply. Connect a 2.2µF or higher value ceramic capacitor from $V_{CCIO}$ to $V_{SSA}$. |
| VCORE | 13 | Power | Internally generated digital I/O 1.8V power supply. Connect a 2.2µF or higher value ceramic capacitor from $V_{CC18}$ to $V_{SSA}$. |
| VCC33 | 16 | Power | Internally generated 3.3V power supply. Connect to a 2.2µF or higher value ceramic capacitor from $V_{CC33}$ to $V_{SSA}$. |
| VSS | 24 | Power | Ground. |
| VM | 34 | Power | High-Voltage Buck Regulator supply controller input. Connect a high value electrolytic capacitor in parallel with a 0.1µF ceramic capacitor from VM to VSS. This pin requires good capacitive bypass to $V_{SS}$, so the ceramic capacitor must be connected with a shorter than 10mm trace from the pin. |
| BST | 35 | Power | High-Voltage Buck Regulator bootstrap input. Connect a 2.2µF or higher value ceramic capacitor from BST to SRC with a shorter than 10mm trace from the pin. |
| DRM | 36 | Power | High-Voltage Buck Regulator Switching supply driver output. Connect to the gate of the external power N-channel MOSFET. |
| SRC | 37 | Power | High-Voltage Buck Regulator Source. Connect to the source of the high-side power MOSFET of the high-voltage buck regulator. |
| VP | 42 | Power | Main power supply. Provides power to the power drivers as well as voltage feedback path for the switching supply. Connect a properly sized supply bypass capacitor in parallel with a 10µF ceramic capacitor in parallel with a 100µF aluminum capacitor from $V_P$ to $V_{SS}$ for voltage loop stabilization. If the switching frequency of the HV-BUCK is >= 200kHz, then the 100µF aluminum capacitor can be replaced with 47µF, but the efficiency will be worse.<br><br>This pin requires good capacitive bypassing to $V_{SS}$, so the ceramic capacitor must be connected with a shorter than 10mm trace from the pin. |
| CSM | 43 | Power | High-Voltage Buck Regulator Switching supply current sense input. Connect to the positive side of the current sense resistor. |
| SW | 47 | Power | Switch node for the medium-voltage buck regulator. |
| VSYS | 48 | Power | 5V System power supply. Connect to a 22µF/6.3V (20%) or higher ceramic capacitor from $V_{SYS}$ to $V_{SS}$. |
| EP (VSS) | EP | Power | Exposed pad. Must be connected to $V_{SS}$ in a star ground configuration. Connect to a large PCB copper area for power dissipation heat sinking. |

## 9.2 Signal Manager Pin Description

| PIN NAME | PIN NUMBER | FUNCTION | TYPE | DESCRIPTION |
|---|---|---|---|---|
| CLKOUT | 17 | CLKOUT | I/O | Low-frequency clock reference output (250Hz – 2kHz), or GPIO. |
| AIO0 | 18 | AIO0 | I/O | Analog front end I/O 0. |
| | | DA0N | Analog | Differential PGA 0 negative input. |
| AIO1 | 19 | AIO1 | I/O | Analog front end I/O 1. |
| | | DA0P | Analog | Differential PGA 0 positive input. |
| AIO2 | 20 | AIO2 | I/O | Analog front end I/O 2. |
| | | DA1N | Analog | Differential PGA 1 negative input. |
| AIO3 | 21 | AIO3 | I/O | Analog front end I/O 3. |

| | | | | |
|---|---|---|---|---|
| | | DA1P | Analog | Differential PGA 1 positive input. |
| AIO4 | 22 | AIO4 | I/O | Analog front end I/O 4. |
| | | DA2N | Analog | Differential PGA 2 negative input. |
| AIO5 | 23 | AIO5 | I/O | Analog front end I/O 5. |
| | | DA2P | Analog | Differential PGA 2 positive input. |
| AIO6 | 38 | AIO6 | I/O | Analog front end I/O 6. |
| | | AMP6 | Analog | PGA input 6. |
| | | CMP6 | Analog | Comparator input 6. |
| | | BUF6 | Analog | Buffer output 6. |
| | | PBTN | Analog | Push button input. |
| AIO7 | 44 | AIO7 | I/O | Analog front end I/O 7. |
| | | AMP7 | Analog | PGA input 7. |
| | | CMP7 | Analog | Comparator input 7. |
| | | PHC7 | Analog | Phase comparator input 7. |
| AIO8 | 45 | AIO8 | I/O | Analog front end I/O 8. |
| | | AMP8 | Analog | PGA input 8. |
| | | CMP8 | Analog | Comparator input 8. |
| | | PHC8 | Analog | Phase comparator input 8. |
| AIO9 | 46 | AIO9 | I/O | Analog front end I/O 9. |
| | | AMP9 | Analog | PGA input 9. |
| | | CMP9 | Analog | Comparator input 9. |
| | | PHC9 | Analog | Phase comparator input 9. |

## 9.3 Driver Manager Pin Description

| PIN NAME | PIN NUMBER | TYPE | DESCRIPTION |
|---|---|---|---|
| DRS3 | 25 | Analog | High-side gate driver source 3. |
| DRH3 | 26 | Analog | High-side gate driver 3. |
| DRB3 | 27 | Analog | High-side gate driver bootstrap 3. Connect a 1µF or higher value ceramic capacitor from DRB3 to DRS3 with a 10mm or shorter trace from the pin. |
| DRS4 | 28 | Analog | High-side gate driver source 4. |
| DRH4 | 29 | Analog | High-side gate driver 4. |
| DRB4 | 30 | Analog | High-side gate driver bootstrap 4. Connect a 1µF or higher value ceramic capacitor from DRB4 to DRS4 with a 10mm or shorter trace from the pin. |
| DRS5 | 31 | Analog | High-side gate driver source 5. |
| DRH5 | 32 | Analog | High-side gate driver 5. |
| DRB5 | 33 | Analog | High-side gate driver bootstrap 5. Connect a 1µF or higher value ceramic capacitor from DRB5 to DRS5 with a 10mm or shorter trace from the pin. |
| DRL0 | 39 | Analog | Low-side gate driver 0. |
| DRL1 | 40 | Analog | Low-side gate driver 1. |
| DRL2 | 41 | Analog | Low-side gate driver 2. |

## 9.4 I/O Ports Pin Description

| PIN NAME | PIN NUMBER | FUNCTION | TYPE | DESCRIPTION[2] |
|---|---|---|---|---|
| PD4 | 1 | PD4 | I/O | I/O port D4. |
| | | PWMD1 | I/O | Timer D PWM/capture 1. |
| PD3 | 2 | PD3 | I/O | I/O port D3. |
| | | PWMA5 | I/O | Timer A PWM/capture 5. |
| | | PWMA7 | I/O | Timer A PWM/capture 7. |
| | | PWMB1 | I/O | Timer B PWM/capture 1. |
| PD2 | 3 | PD2 | I/O | I/O port D2. |
| | | PWMA3 | I/O | Timer A PWM/capture 3. |
| | | PWMA4 | I/O | Timer A PWM/capture 4. |
| | | PWMB0 | I/O | Timer B PWM/capture 0. |
| PD1 | 4 | PD1 | I/O | I/O port D1. |
| | | SWDCL | I | Serial wire debug clock. |
| | | EXTCLK | I | External clock input. |
| PD0 | 5 | PD0 | I/O | I/O port D0. |
| | | SWDIO | I/O | Serial wire debug I/O. |
| PE0 | 6 | PE0 | I/O | I/O port E0. |
| | | SPICLK | I/O | SPI clock. |
| PE1 | 7 | PE1 | I/O | I/O port E1. |
| | | SPIMOSI | I/O | SPI master out, slave in (MOSI) |
| | | UARTTX | O | UART transmit output. |
| PE2 | 8 | PE2 | I/O | I/O port E2. |
| | | SPI MISO | I/O | SPI master in, slave out (MISO) |
| | | UARTRX | I | UART receive input. |
| PE3 | 9 | PE3 | I/O | I/O port E3. |
| | | SPICS0 | O | SPI chip select 0. |
| | | nRESET1 | I | Reset input 1. |
| PE4 | 10 | PE4 | I/O | I/O port E4. |
| | | SPICS1 | O | SPI chip select 1. |
| | | I2CSCL | I/O | I2C clock |
| PE5 | 11 | PE5 | I/O | I/O port E5. |
| | | SPICS2 | O | SPI chip select 2. |
| | | I2CSDA | I/O | I2C data. |
| PC3 | 14 | PC3 | I/O | I/O port C3. |
| | | AD3 | Analog | ADC input 3. |
| PC2 | 15 | PC2 | I/O | I/O port C2. |
| | | AD2 | Analog | ADC input 2. |

[2] For a full description of all of the pin configurations for each digital I/O, see the PAC5232 User Guide for the Peripheral MUX.

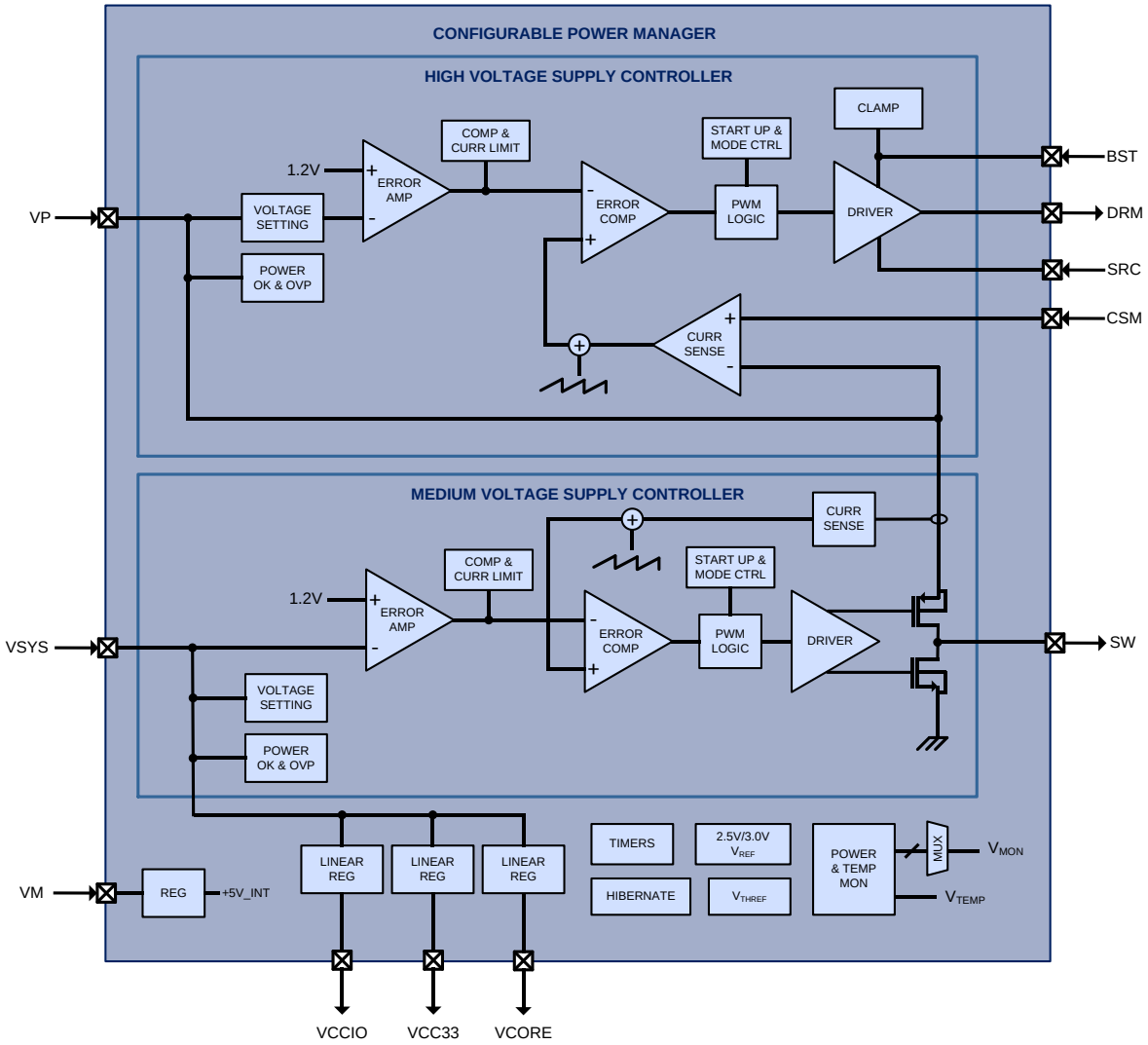
| | | | | |
|---|---|---|---|---|
| PD7 | 49 | PD7 | I/O | I/O port D7. |
| | | PWMA6 | I/O | Timer A PWM/capture 6. |
| | | PWMD0 | I/O | Timer D PWM/capture 0. |
| PD6 | 50 | PD6 | I/O | I/O port D6. |
| | | PWMA7 | I/O | Timer A PWM/capture 7. |
| | | PWMB1 | I/O | Timer B PWM/capture 1. |
| PD5 | 51 | PD5 | I/O | I/O port D5. |
| | | PWMA5 | I/O | Timer A PWM/capture 5. |
| | | PWMC1 | I/O | Timer C PWM/capture 1. |

# 10 CONFIGURABLE POWER MANAGER (CPM)

## 10.1 Features

- 160V Buck DC/DC Controller (HV Buck)
  - 25V – 160V input
- 5V Switching Regulator (MV Buck)
- 3 linear regulators with power and hibernate management, including $V_{REF}$ for ADC
- Power and temperature monitor, warning, and fault detection

**Figure 10-1 CPM Block Diagram**



## 10.2 Functional Description

The Configurable Power Manager (Figure 10-1) is optimized to efficiently provide “all-in-one” power management required by the PAC® and associated application circuitry. It incorporates a high-voltage power supply controller that is used to convert power from a DC input source to generate a main supply output $V_P$. There is also an integrated medium-voltage buck DC/DC regulator to generate $V_{SYS}$.

Three other linear regulators provide $V_{CCIO}$, $V_{CC33}$, and $V_{CORE}$ supplies for 3.3V I/O, 3.3V mixed signal, and 1.9V microcontroller core circuitry. The power manager also handles system functions including internal reference generation, timers, hibernate mode management, and power and temperature monitoring.

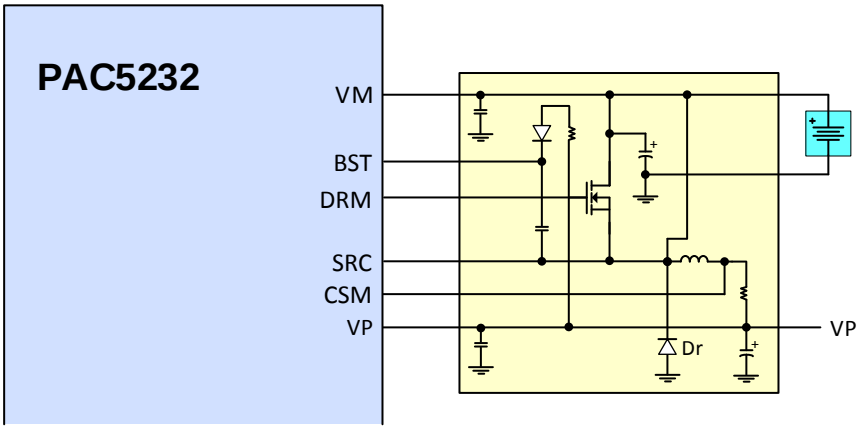
## 10.3 High-Voltage Supply Controller (HV-BUCK)

The PAC5232 contains a High-Voltage Supply Controller for a Buck DC/DC. This power supply is used to supply the various regulators in the PAC5232, as generating the $V_P$ gate drive voltage for the Application Specific Driver Manager (ASPD).

The HV-BUCK controller drives an external power MOSFET for pulse-width modulation switching of an inductor or transformer for power conversion. The VM is the HV-BUCK supply controller input. The DRM output drives the gate of the N-CH MOSFET between the $V_M$ on state and $V_{SS}$ off state at proper duty cycle and switching frequency to ensure that the main supply voltage $V_P$ is regulated. The gate of the high-side power MOSFET is connected to the DRM pin and the source of the high-side power MOSFET is connected to SRC.

The $V_P$ regulation voltage is initially set to 12V during start up, and can be reconfigured to be 15V by the microcontroller after initialization. When $V_P$ is lower than the target regulation voltage, the internal feedback control circuitry causes the inductor current to increase to raise $V_P$. Conversely, when $V_P$ is higher than the regulation voltage, the feedback loop control causes the inductor current to decrease to lower $V_P$. The feedback loop is internally stabilized. The output current capability of the switching supply is determined by the external current sense resistor. The inductor current signal is sensed differentially between the CSM pin and $V_P$, and has a peak current limit threshold of 0.2V.

**Figure 10-2 HV-BUCK Example**




The switching frequency and output voltage of the HV-BUCK can be reconfigured by the MCU. The switching frequency can be configured to be between 50kHz and 400kHz and the gate drive output voltage can be configured to either 12V or 15V to work for a range of MOSFET or IGBT based inverters.

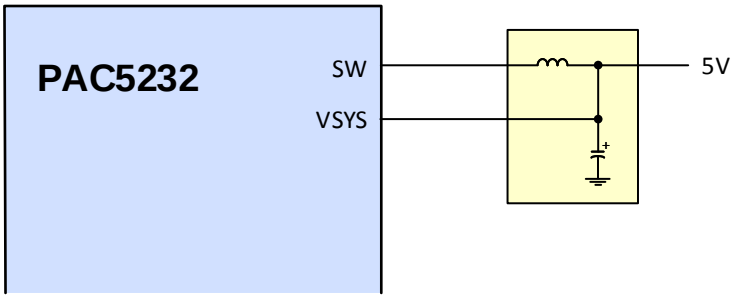
The Rectifier Diode (Dr) must be a low QRR diode.

## 10.4 Medium-Voltage Buck Regulator (MV-BUCK)

The PAC5232 contains a Medium-Voltage Buck Switching Regulator that generates a 5V, 200mA supply for the device, as well as PCB functions.

The SW pin is the switch node of the Buck regulator. The Power MOSFET is integrated, so connect this pin to VSYS through an external inductor. The VSYS pin is the 5V regulator output, which should be bypassed to ground.

**Figure 10-3 MV-BUCK Switching Regulator Example**

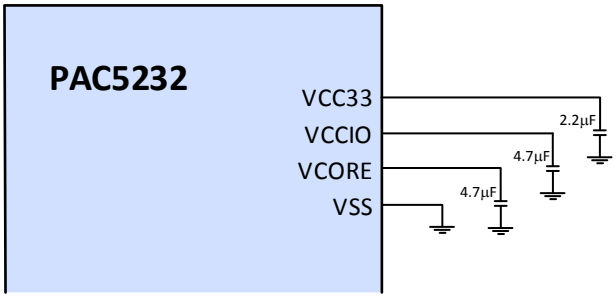



The output of VSYS is fixed at 5V and the switching frequency is 1.33MHz. This regulator supplies at least 200mA. This buck regulator offers better thermal and efficiency performance.

## 10.5 Linear Regulators

The CPM includes three additional linear regulators. VSYS supplies these three regulators. Once VSYS is above 4.5V, these three additional 40mA linear regulators for VCCIO, VCC33, and VCORE supplies sequentially power up.

**Figure 10-4 Linear Regulators Example**



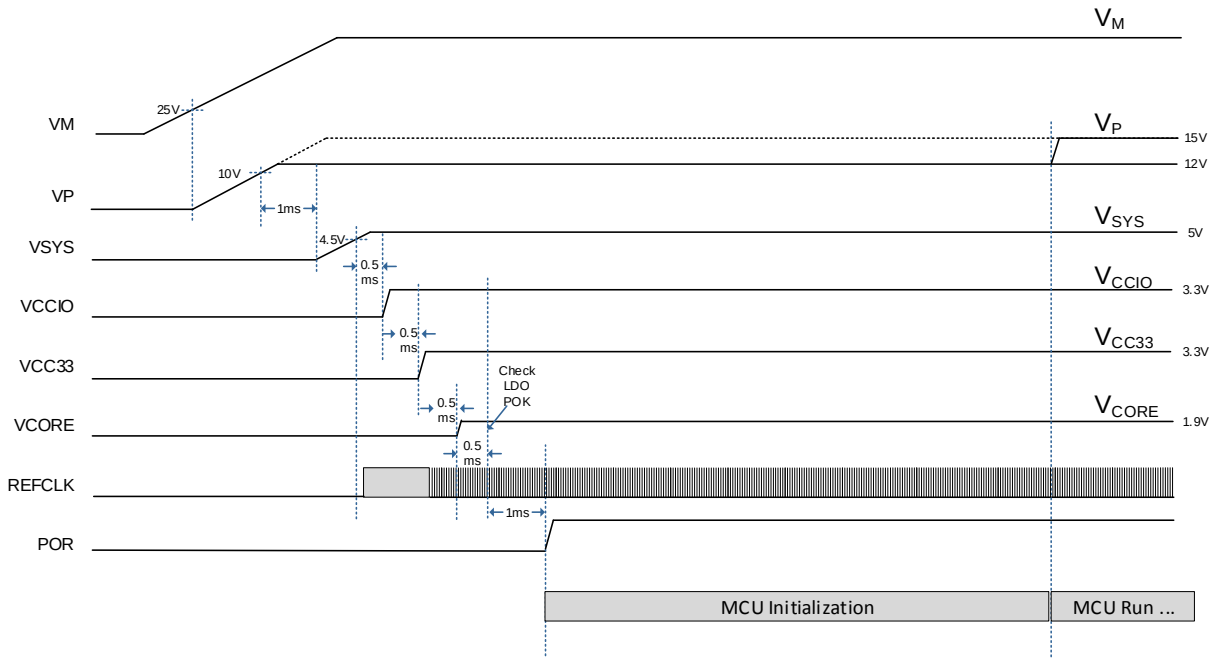

The figure above shows typical circuit connections for the linear regulators. The VCCIO regulator generates a dedicated 3.3V supply for IO. The VCC33 and VCORE regulators generate 3.3V and 1.9V, respectively. When VSYS, VCCIO, VCC33, and VCORE are all above their respective power good thresholds, and the configurable power on reset duration has expired, the microcontroller is initialized.[3]

[3] Note that the VCORE LDO may not have any addition load on it from the PCB. The only components connected to VCORE should be a bypass capacitor to ground.

## 10.6 Power-up Sequence

The CPM follows a typical power up sequence as in the Figure 10-5 below.

**Figure 10-5 Power-Up Sequence**




A typical sequence begins with motor power supply (VM) being applied and rising to 25V. When VM rises to 25V, the HV-BUCK controller is started and VP starts to rise. When VP rises over the UVLO rising threshold, then there is a 1ms delay and then the MV-BUCK is enabled. When VSYS rises to 4.5V, then there is a 0.5ms delay and the VCCIO LDO is enabled. Then there is a 0.5ms delay and the VCC33 LDO is enabled. Then there is a 0.5ms delay and the VCORE LDO is enabled.

There is then a 0.5ms delay and the power good threshold of all LDOs is checked. If all are OK, then there is an additional 1ms delay, then the POR signal is asserted to the MCU and it begins executing firmware.

During the firmware initialization process, the MCU may change the VP output voltage setting from the 12V default to 15V.

## 10.7 Hibernate Mode

The IC can go into an ultra-low power hibernate mode via the microcontroller firmware or via the optional push button (PBTN, see *Push Button* description in *Configurable Analog Front End*). In hibernate mode, only a minimal amount (typically 19µA at 56V) of current is used by $V_M$, and the CPM controller and all internal regulators are shut down to eliminate power drain from the output supplies. The system exits hibernate mode after a wake-up timer duration (configurable from 125ms to 8s or infinite) has expired or, if push button enabled, after an additional push button event has been detected. When exiting the hibernate mode, the power manager goes through the start up cycle and the microcontroller is reinitialized. Only the persistent power manager status bits (resets and faults) are retained during hibernation.

## 10.8 Power and Temperature Monitor

Whenever any of the $V_{SYS}$, $V_{CCIO}$, $V_{CC33}$, or $V_{CORE}$ power supplies falls below their respective power good threshold voltage, a fault event is detected and the microcontroller is reset. The microcontroller stays in the reset state until $V_{SYS}$, $V_{CCIO}$, $V_{CC33}$, and $V_{CC18}$ supply rails are all good again and the reset time has expired. A microcontroller reset can also be initiated by a maskable temperature fault event that occurs when the IC temperature reaches 165°C. The fault status bits are persistent during reset, and can be read by the microcontroller upon re-initialization to determine the cause of previous reset.

A power monitoring signal $V_{MON}$ is provided onto the ADC pre-multiplexer for monitoring various internal power supplies. $V_{MON}$ can be set to be $V_{CORE}$, 0.4•$V_{CORE}$, 0.4•$V_{CC33}$, 0.4•$V_{CCIO}$, 0.4•$V_{SYS}$, 0.1•$V_P$, or the internal compensation voltage $V_{COMP}$ for switching supply power monitoring.

For power and temperature warning, an IC temperature warning event at 140°C are provided as a maskable interrupt to the microcontroller. This warning allows the microcontroller to safely power down the system.

In addition to the temperature warning interrupt and fault reset, a temperature monitor signal is provided onto the ADC pre-multiplexer for IC temperature measurement.

This value has a compensation coefficient available in INFO FLASH that can be used to obatin an accurate temperature. The parameter VT300K will be stored in INFO FLASH and will indicate the compensation factor.

The temperature can then be obatined by the following formula:

$V_{TEMP\_KELVIN}$ = 300 * (VM + 0.075) / (VT300K + 0.075)

For information on on the location of this temperature coefficient, see the PAC5232 User Guide.

## 10.9 Voltage Reference

The reference block includes a 1.2V high-precision reference voltage used internally and for all the LDOs. There is also a high-accuracy 2.5V reference for the ADC $V_{REF}$ on the MCU. There is also a 4-level programmable threshold voltage $V_{THREF}$ (0.1V, 0.2V, 0.5V, and 1.25V).

## 10.10 Electrical Characteristics

### Table 10-1 High-Voltage Buck Controller Electrical Characteristics

($V_M$ = 30V, $V_P$ = 12V and $T_J$ = 25°C unless otherwise specified)

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_{HIB;VM}$ | $V_M$ hibernate mode supply current | Hibernate mode, VM = 56V | | 19 | 26 | µA |
| | | Hibernate mode, VM = 80V | | 22.5 | | µA |
| $V_{UVLOR;VM}$ | $V_M$ UVLO rising | | 23 | 25 | 27 | V |
| $V_{UVLOF;VM}$ | $V_M$ UVLO hysteresis | | | 2 | | V |
| $V_{REF;VP}$ | $V_P$ output regulation voltage | Set to 12V | -5% | 12 | -5% | V |
| $k_{POKR;VP}$ | $V_P$ power OK threshold | $V_P$ rising | | 91 | | % |
| $k_{POKF;VP}$ | | $V_P$ falling | | 87 | | % |
| $k_{OVPR;VP}$ | $V_P$ OV protection threshold | $V_P$ rising, blanking = 10µs | | 130 | | % |
| $t_{ONMIN;DRM}$ | DRM minimum on time | | 90 | 200 | 300 | ns |
| $t_{OFFMIN;DRM}$ | DRM minimum off time | | 390 | 600 | 1150 | ns |
| $V_{UVLOR;VP}$ | $V_P$ UVLO rising | | | 10 | | V |
| $V_{UVLOF;VP}$ | $V_P$ UVLO falling | | | 8 | | V |
| $V_{CSM;ILIM}$ | CSM current limit threshold | | -12% | 0.2 | 12% | V |
| $F_{S;DRM}$ | Switching frequency | Frequency setting: 50kHz, 100kHz (default), 200kHz, 400kHz | -5 | | 5 | % |
| $I_{SOURCE;DRM}$ | DRM output high source current | | | 100 | | mA |
| $I_{SINK;DRM}$ | DRM output low sink current | | | 200 | | mA |
| | HV-BUCK inductor value | | | 100 | | µH |
| $I_{DSG}$ | Discharge current | | | 10 | | mA |
| $V_{VM}$ | Motor voltage range | | 0 | | 160 | V |
| $V_{SRC;VSS}$ | SRC to ground range | | -10 | | VM + 10 | V |
| $V_{SRC;VM}$ | SRC to VM range | | | | 10 | V |
| $V_{BST;VSS}$ | BST to ground range | | | | 175 | V |

### Table 10-2 Medium-Voltage Buck Controller Electrical Characteristics

($V_M$ = 30V, $V_P$ = 12V and $T_J$ = 25°C unless otherwise specified)

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{VSYS}$ | $V_{SYS}$ output voltage accuracy | | -3% | 5 | 3% | V |
| $F_{SW}$ | Switching frequency | | -5% | 1.33 | 5% | MHz |
| $I_{VSYS;LIM}$ | $V_{SYS}$ current limit | | 420 | | 550 | mA |
| $I_{VSYS}$ | $V_{SYS}$ output current | $V_{SYS}$ > 3V | 200 | | | mA |
| | | $V_{SYS}$ < 2.5V | 100 | | | mA |
| $V_{POK;VSYS}$ | $V_{SYS}$ power OK threshold | Rising | 4.25 | 4.5 | 4.75 | V |
| | | Falling | | 4.2 | | V |
| | $V_{SYS}$ power OK blanking delay | | | 10 | | µs |
| | MV-BUCK inductor value | Current rating of at least 750mA | 6.8 – 20% | | 10 + 20% | µH |
| $V_{UVLO;VSYS}$ | $V_{SYS}$ UVLO | Rising | | 4.5 | | V |
| | | Falling | | 4.2 | | V |
| $V_{OVP;VSYS}$ | $V_{SYS}$ OVP | Rising | | 5.5 | | V |
| | | Falling | | 5.2 | | V |

### Table 10-3 Linear Regulators Electrical Characteristics

($V_P$ = 12V and $T_A$ = -40°C to 105°C unless otherwise specified)

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{CCIO}$ | $V_{CCIO}$ output voltage | Load = 1mA | -3% | 3.3 | 3% | V |
| $V_{CCIO}$ | $V_{CCIO}$ output voltage | Load = 1mA | -3% | 3.3 | 3% | V |
| $V_{CORE}$[4] | $V_{CORE}$ output voltage | Load = 1mA | -3% | 1.9 | 3% | V |
| $I_{LIM;VCCIO}$ | $V_{CCIO}$ current limit | | 40 | 65 | | mA |
| $I_{LIM;VCC33}$ | $V_{CC33}$ current limit | | 40 | 65 | | mA |
| $I_{LIM;VCORE}$ | $V_{CORE}$ current limit | | 40 | 65 | | mA |
| | LDO current fold back | | | 50 | | % |
| $t_{POK;BLANK}$ | Power OK blanking delay | $V_{CCIO}$, $V_{CC33}$, $V_{CORE}$ | | 10 | | µs |
| $R_{DISCH}$ | Output discharge resistance | LDO off | | 300 | | Ohm |
| $C_{VCCIO}$ | VCCIO stable output capacitance | | 1 | | 4.7 | µF |
| $C_{VCC33}$ | VCC33 stable output capacitance | | 1 | | 4.7 | µF |
| $C_{VCORE}$ | VCORE stable output capacitance | | 1 | | 4.7 | µF |
| $V_{LDO;POK}$ | LDO power OK rising threshold | Hysteresis = 10% | 85 | 90 | 95 | % |

[4] Note that the VCORE LDO may not have any other loads. The only connection to the VCORE pin should be a bypass capacitor to ground.

## 10.11 Typical Performance Characteristics

**($T_A$ = 25ºC unless otherwise specified)**

**Figure 10-6 VDDIO LDO Voltage vs. Current**

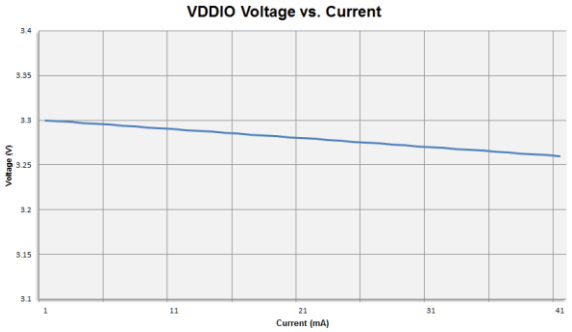



**Figure 10-7 VCC33 LDO Voltage vs. Current**

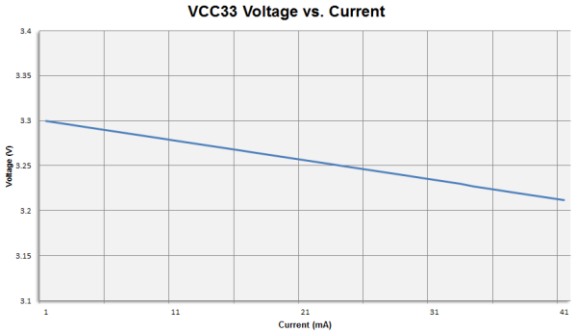
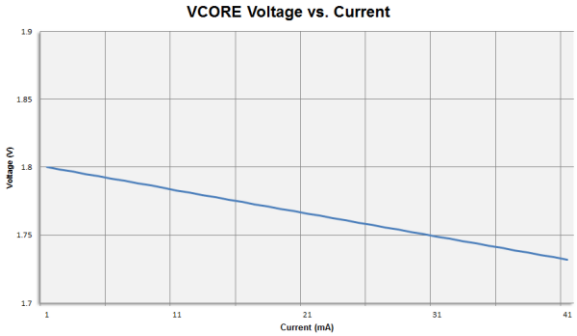



**Figure 10-8 VCORE LDO Voltage vs. Current**



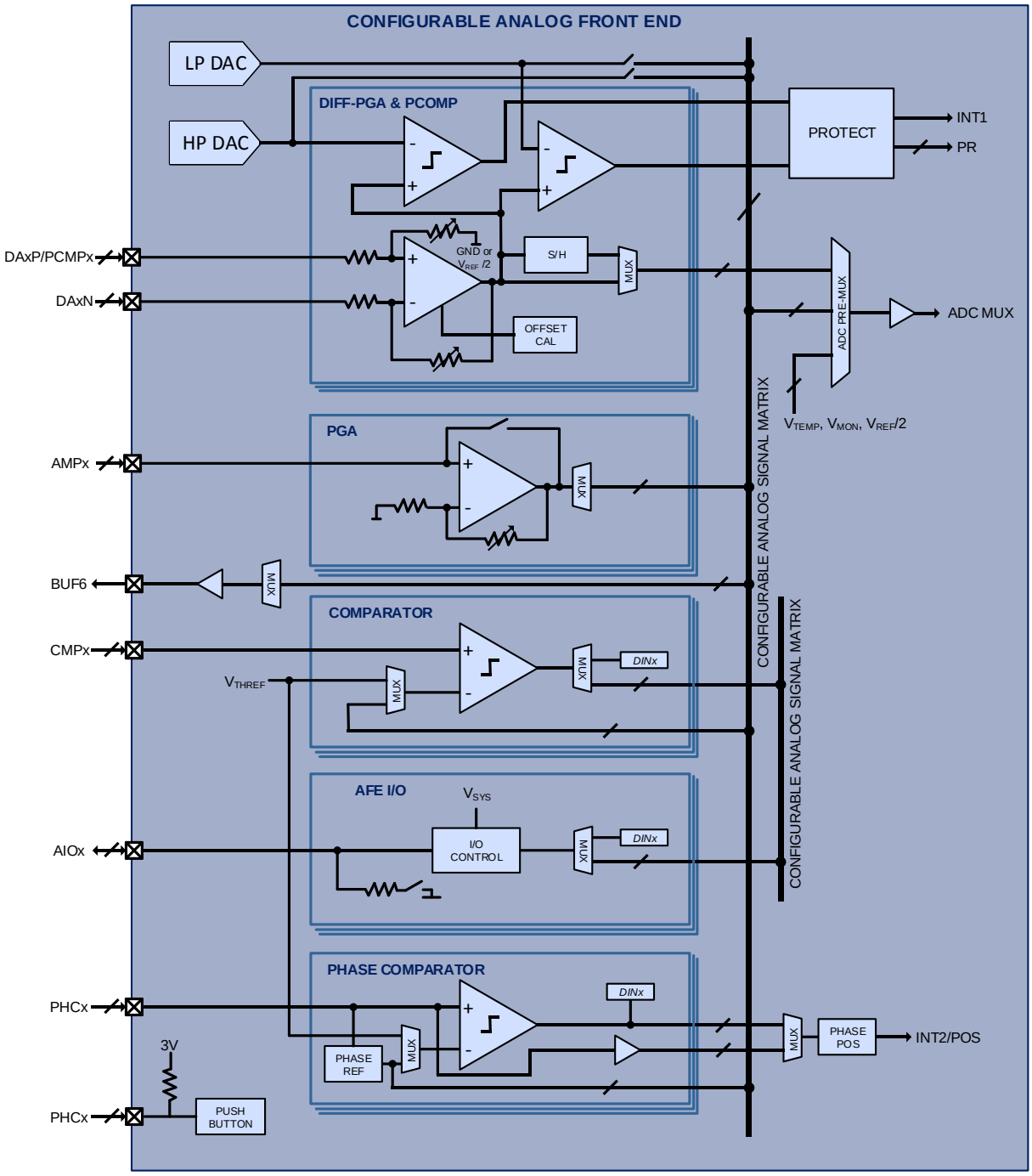
# 11 CONFIGURABLE ANALOG FRONT END (CAFE)

## 11.1 Features

- 10 Configurable Analog I/O signals
  - Gain mode, comparator mode, I/O mode, special mode
- 3 High-Performance, Configurable Differential Amplifiers
- 4 High-Performance, Configurable Single-Ended Amplifiers
- Two high-speed comparators with protection functions
- Phase to phase, phase to center-tap modes
- Bi-directional, asymmetric configurable comparator hysteresis
- Push-button input for entering/exiting hibernate mode
- Low-frequency Clock Output for safety applications

## 11.2 Block Diagram

**Figure 11-1 Configurable Analog Front End**



## 11.3 Functional Description

The device includes a Configurable Analog Front End (CAFE, Figure 11-1) accessible through 8 analog and I/O pins. These pins can be configured to form flexible interconnected circuitry made up of 3 differential programmable gain amplifiers, 4 single-ended programmable gain amplifiers, 4 general purpose comparators, 3 phase comparators, 10 protection comparators, and one buffer output. These pins can also be programmed as analog feed-through pins, or as analog front end I/O pins that can function as digital inputs or digital open-drain outputs. The PAC® proprietary configurable analog signal matrix (CASM) and configurable digital signal matrix (CDSM) allow real time asynchronous analog and digital signals to be routed in flexible circuit connections for different applications. A push button function is provided for optional push button on, hibernate, and off power management function.

## 11.4 Differential Programmable Gain Amplifier (DA)

The DAxP and DAxN pin pair are positive and negative inputs, respectively, to a differential programmable gain amplifier. The differential gain can be programmable to be 1x, 2x, 4x, 8x, 16x, 32x, and 48x for zero ohm signal source impedance. The differential programmable gain amplifier has -0.3V to 2.5V input common mode range, and its output can be configured for routing directly to the ADC pre-multiplexer, or through a sample-and-hold circuit synchronized with the ADC auto-sampling mechanism. Each differential amplifier is accompanied by offset calibration circuitry, and two protection comparators for protection event monitoring. The programmable gain differential amplifier is optimized for use with signal source impedance lower than 500Ω and with matched source impedance on both positive and negative inputs for minimal offset. The effective gain is scaled by 13.5k / (13.5k + $R_{SOURCE}$), where $R_{SOURCE}$ is the matched source impedance of each input.

## 11.5 Single-Ended Programmable Gain Amplifier (AMP)

Each AMPx input goes to a single-ended programmable gain amplifier with signal relative to $V_{SS}$. The amplifier gain can be programmed to be 1x, 2x, 4x, 8x, 16x, 32x, and 48x, or as analog feed-through. The programmable gain amplifier output is routed via a multiplexer to the configurable analog signal matrix CASM.

## 11.6 General Purpose Comparator (CMP)

The general purpose comparator takes the CMPx input and compares it to either the programmable threshold voltage ($V_{THREF}$) or a signal from the configurable analog signal matrix CASM. The comparator has 0V to $V_{SYS}$ input common mode range, and its polarity-selectable output is routed via a multiplexer to either a data input bit or the configurable digital signal matrix CDSM. Each general purpose comparator has two mask bits to prevent or allow rising or falling edge of its output to trigger second microcontroller interrupt INT2, where INT2 can be configured to active protection event PR.

## 11.7 Phase Comparator (PHC)

The phase comparator takes the PHCx input and compares it to either the programmable threshold voltage ($V_{THREF}$) or a signal from the configurable analog signal matrix CASM. The comparison signal can be set to a phase reference signal generated by averaging the PHCx input voltages. In a three-phase motor control application, the phase reference signal acts as a virtual center tap for BEMF detection. The PHCx inputs are optionally fed through to the CASM. The PHC inputs can be compared to the virtual center-tap, or phase to phase for the most efficient BEMF zero-cross detection.

The phase comparator signals can also be configured to the other two phase comparators (between AIO7, AIO8 and AIO9), to perform phase to phase comparisons.

The comparator blanking time is configurable. The blanking time configuration supports bi-directional and asymmetric configurations, which enables hysteresis for rising and falling signals.

The phase comparator has 0V to $V_{SYS}$ input common mode range, and its polarity-selectable output is routed to a data input bit and to the phase/position multiplexer synchronized with the auto-sampling sequencers.

## 11.8 Protection Comparator (PCMP)

Two protection comparators are provided in association with each differential programmable gain amplifier, with outputs available to trigger protection events and accessible as read-back output bits. The HP comparator compares the amplifier output to the 10-bit HP DAC output voltage, with full scale voltage of 2.5V. The limit protection (LP) comparator compares the differential programmable gain amplifier output to the 10-bit LP DAC output voltage, with full scale voltage of 2.5V.

Each protection comparator has a mask bit to prevent or allow it to trigger the main microcontroller interrupt INT1. Each protection comparator also has one mask bit to prevent or allow it to activate protection event PR. These two protection events can be used directly by protection circuitry in the Application Specific Power Drivers (ASPD) to protect devices being driven.

## 11.9 Analog Output Buffer (BUF)

A subset of the signals from the configurable analog signal matrix CASM can be multiplexed to the BUF6 pin for external use. The buffer offset voltage can be minimized with the built-in swap function.

## 11.10 Analog Front End I/O (AIO)

The PAC5232 has 10 AIOx pins that are available. In the analog front end I/O mode, the pin can be configured to be a digital input or digital open-drain output. The AIOx input or output signal can be set to a data input or output register bit, or multiplexed to one of the signals in the configurable digital signal matrix CDSM. The signal can be set to active high (default) or active low, with $V_{SYS}$ supply rail. Where $AIO_{6,7,8,9}$ supports microcontroller interrupt for external signals. Each has two mask bits to prevent or allow rising or falling edge of its corresponding digital input to trigger second microcontroller interrupt INT2.

## 11.11 Push Button (PBTN)

The push button PBTN, when enabled, can be used by the MCU to detect a user active-low push button event and to put the system into an ultra-low-power hibernate mode. Once the system is in hibernate mode, PBTN can be used to wake up the system.

In addition, PBTN can also be used as a hardware reset for the microcontroller when it is held low for longer than 8s during normal operation. The PBTN input is active low and has a 55kΩ pull-up resistor to 3V.

## 11.12 HP DAC and LP DAC

The 10-bit HP DAC can be used as the comparison voltage for the high-speed protection (HP) comparators, or routed for general purpose use via the AB2 signal in the CASM. The HP DAC output full scale voltage is 2.5V.

The 10-bit LP DAC can be used as the comparison voltage for the limit protection (LP) comparators, or routed for general purpose use via the AB3 signal in the CASM. The LP DAC output full scale voltage is 2.5V.

## 11.13 ADC Pre-Multiplexer

The ADC pre-multiplexer is a 16-to-1 multiplexer that selects between the 3 differential programmable gain amplifier outputs, AB1 through AB9, temperature monitor signal ($V_{TEMP}$), power monitor signal ($V_{MON}$), and offset calibration reference ($V_{REF}$ / 2). The ADC pre-multiplexer can be directly controlled or automatically scanned by the auto-sampling sequencer.

When the ADC pre-multiplexer is automatically scanned, the unbuffered or sensitive signals should be masked by setting appropriate register bits.

## 11.14 Configurable Analog Signal Matrix (CASM)

The CASM has 9 general purpose analog signals labeled AB1 through AB9 that can be used for:

- Routing the single-ended programmable gain amplifier or analog feed-through output to AB1 through AB9
- Routing an analog signal via AB1, AB2, or AB3 to the negative input of a general purpose comparator or phase comparator
- Routing the 10-bit HP DAC output to AB2
- Routing the 10-bit LP DAC output to AB3
- Routing analog signals via AB1 through AB12 to the ADC pre-multiplexer
- Routing phase comparator feed-through signals to AB7, AB8, and AB9, and averaged voltage to AB1

## 11.15 Configurable Digital Signal Matrix (CDSM)

The CDSM has 7 general purpose bi-directional digital signals labeled DB1 through DB7 that can be used for:

- Routing the AIOx input to or output signals from DB1 through DB7
- Routing the general purpose comparator output signals to DB1 through DB7

## 11.16 Low-Frequency Clock Output

The PAC5232 has a configurable low-frequency clock output. When enabled, the device will output a 250Hz, 50% duty cycle clock to the CLKOUT pin.

The supported clock frequencies are 250Hz, 500Hz, 1kHz or 2kHz.

## 11.17 Cycle-by-cycle Current Limit

The PAC5232 contains hardware support for cycle by cycle current limit. The user may configure this feature to use the LPCOMP DAC as the current threshold. The CAFE will automatically perform duty cycle truncation to lower current at any time the associated phase current is greater than the setting of the LPCOMP DAC.

## 11.18 Temperature Protection

The PAC5232 contains an internal temperature sensor that detects temperature warnings and faults.

When the device temperature reaches the temperature warning threshold (140ºC), the device sets an over-temperature warning condition. The user may configure a mask-able interrupt the MCU for this condition.

When the device temperature reaches the temperature fault threshold (165 ºC), the device is shut down. There is no interrupt for this condition.

For more details on the register settings for over-temperature protection see the PAC5232 User Guide and related application notes.

## 11.19 Electrical Characteristics

### Table 11-1 Differential Programmable Gain Amplifier (DA) Electrical Characteristics (AIO<5:0>)

($T_A$ = -40°C to 105°C unless otherwise specified.)

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{ICMR;DA}$ | Input common mode range | | -0.3 | | 2.5 | V |
| $I_{CC;DA}$ | Operating supply current | Each enabled amplifier | | 150 | | μA |
| $V_{OS;DA}$ | Input offset voltage | Gain = 8x | -8 | | 8 | mV |
| $k_{CMRR;DA}$ | Common mode rejection ratio | | 50 | 80 | | dB |
| | Slew rate | Gain = 8x | 10 | | | V/μs |
| $R_{INDIF;DA}$ | Differential input impedance | | | 27 | | kΩ |
| $t_{ST;DA}$ | Settling time | To 1% of final value | | | 360 | ns |
| $A_{VZI;DA}$ | Differential amplifier gain (zero ohm source impedance) | Gain = 1x | | 1 | | % |
| | | Gain = 2x | | 2 | | |
| | | Gain = 4x | | 4 | | |
| | | Gain = 8x, $V_{DAxP}$=$V_{DAxN}$=0V, $T_A$ = 25°C | -2 | | 2 | |
| | | Gain = 16x | | 16 | | |
| | | Gain = 32x | | 32 | | |
| | | Gain = 48x | | 48 | | |

### Table 11-2 Single-Ended Programmable Gain Amplifier (AMP) Electrical Characteristics (AIO<9:6>)

($V_{SYS}$ = 5V, $V_{CCIO}$ = 3.3V and $T_A$ = -40°C to 105°C unless otherwise specified.)

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{ICMR;AMP}$ | Input common mode range | | 0 | | $V_{SYS}$ | V |
| $I_{CC;AMP}$ | Operating supply current | Each enabled amplifier | | 80 | 120 | μA |
| $V_{OS;AMP}$ | Input offset voltage | Gain = 8x | -10 | | 10 | mV |
| | Slew rate | Gain = 1x | 10 | | | V/μs |
| $t_{ST;AMP}$ | Settling time | To 1% of final value | | | 360 | ns |
| $V_{OLR;AMP}$ | Output linear range | | 0.1 | | 2.5 | V |
| $A_{V;AMP}$ | Amplifier gain | Gain = 1x | | 1 | | % |
| | | Gain = 2x | | 2 | | |
| | | Gain = 4x | | 4 | | |
| | | Gain = 8x, $V_{AMPx}$=125mV, $T_A$ = 25°C | -2 | | 2 | |
| | | Gain = 16x | | 16 | | |
| | | Gain = 32x | | 32 | | |
| | | Gain = 48x | | 48 | | |
| | | | | | | |

| | | | | | | |
|---|---|---|---|---|---|---|
| $t_{ST;AMP}$ | Settling time | To 1% of final value | | | 350 | ns |

### Table 11-3 General Purpose Comparator (CMP) Electrical Characteristics (AIO<9:6>)

($T_A$ = -40°C to 105°C unless otherwise specified.)

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{ICMR;CMP}$ | Input common mode range | | 0 | | $V_{SYS}$ | V |
| $I_{CC;CMP}$ | Operating supply current | Each enabled comparator | | 35 | | µA |
| $V_{OS;CMP}$ | Input offset voltage | | -10 | | 10 | mV |
| $V_{HYS;CMP}$ | Hysteresis | | | 22 | | mV |
| $t_{DEL;CMP}$ | Comparator delay | | | | 1 | µs |
| $t_{DELMODE;CMP}$ | Mode change blanking delay | | | 10 | | µs |

### Table 11-4 Phase Comparator (PHC) Electrical Characteristics (AIO<9:6>)

($V_{SYS}$ = 5V, $V_{CC33}$ = 3.3V and $T_A$ = -40°C to 105°C unless otherwise specified.)

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{ICMR;PHC}$ | Input common mode range | | | | | V |
| $I_{CC;PHC}$ | Operating supply current | Each enabled comparator | | 35 | | µA |
| $V_{OS;PHC}$ | Input offset voltage | | -10 | | 10 | mV |
| $V_{HYS;PHC}$ | Hysteresis | | | 23 | | mV |
| $t_{DEL;PHC}$ | Comparator delay | 10mV difference input | | | 1 | µs |

### Table 11-5 Special Mode Electrical Characteristics (AIO<9:7>)

($T_A$ = -40°C to 105°C unless otherwise specified.)

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{ICMR;SPEC}$ | Input common mode range | | 0 | | $V_{SYS}$ | V |
| $I_{CC;SPEC}$ | Operating supply current | Each enabled comparator | | 80 | 120 | µA |
| $V_{HSYS;SPEC}$ | Comparator Hysteresis, HYSMODE = 0 | AIO<9:7>HYS = 00b (0mV) | | 0 | | mV |
| | | AIO<9:7>HYS = 01b (6mV) | 4 | 6 | 8 | mV |
| | | AIO<9:7>HYS = 10b (12mV) | 9 | 12 | 15 | mV |
| | | AIO<9:7>HYS = 11b (24mV) | 18 | 24 | 30 | mV |
| | Comparator Hysteresis, HYSMODE = 1 | AIO<9:7>HYS = 00b (0mV) | | 0 | | mV |
| | | AIO<9:7>HYS = 01b (24mV) | 18 | 24 | 30 | mV |
| | | AIO<9:7>HYS = 10b (48mV) | 36 | 48 | 60 | mV |
| | | AIO<9:7>HYS = 11b (96mV) | 72 | 96 | 120 | mV |

### Table 11-6 Special Mode Electrical Characteristics (AIO6)

($T_A$ = -40°C to 105°C unless otherwise specified.)

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{ICMR;SPEC}$ | Input common mode range | | 0 | | $V_{SYS}$ | V |
| $I_{CC;SPEC6}$ | Operating supply current | | | 60 | | µA |
| $V_{INOFF;SPEC6}$ | Input offset voltage | | -20 | | 20 | mV |
| $I_{OUT;SPEC6}$ | Output current | | | 2 | | mA |

### Table 11-7 Analog Front End (AIO) Electrical Characteristics (AIO<9:0>)

($T_A$ = -40°C to 105°C unless otherwise specified.)

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{AIO}$ | Pin voltage range | | 0 | | 5 | V |
| $V_{IH;AIO}$ | High-level input voltage | | 2.2 | | | V |
| $V_{IL;AIO}$ | Low-level input voltage | | | | 0.8 | V |
| $R_{PD;AIO}$ | Pull-down resistance | Input mode | | 1 | | MΩ |
| $V_{OL;AIO}$ | Low-level output voltage | $I_{AIOx}$=7mA, open-drain output mode | | | 0.3 | V |
| $I_{OL;AIO}$ | Low-level output sink current | $V_{AIOx}$ = 0.4V, open-drain output mode | 6 | 14 | | mA |
| $I_{LK;AIO}$ | High-level output leakage current | $V_{AIOx}$ = 5V, open-drain output mode | | 0 | 10 | µA |

### Table 11-8 Push Button (PBTN) Electrical Characteristics (AIO6)

($T_A$ = -40°C to 105°C unless otherwise specified.)

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{I;PBTN}$ | Input voltage range | | 0 | | 5 | V |
| $V_{IH;PBTN}$ | High-level input voltage | | 2.2 | | | V |
| $V_{IL;PBTN}$ | Low-level input voltage | | | | 0.8 | V |
| $R_{PU;PBTN}$ | Pull-up resistance | To 3V, push-button input mode | | 50 | | kΩ |

### Table 11-9 HP DAC and LP DAC Electrical Characteristics

($T_A$ = -40°C to 105°C unless otherwise specified.)

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{DACREF}$ | DAC reference voltage | TA = 25°C | -0.5% | 2.5 | 0.5% | V |
| | | TA = -40°C to 105°C | -0.9% | 2.5 | 0.9% | |
| | HP 10-bit DAN INL | | -2 | | 2 | LSB |
| | HP 10-bit DAC DNL | | -0.5 | | 0.5 | LSB |
| | LP 10-bit DAC INL | | -2 | | 2 | LSB |
| | LP 10-bit DAC DNL | | -0.5 | | 0.5 | LSB |

### Table 11-10 Low-Frequency Clock Output (CLKOUT)

($T_A$ = -40°C to 105°C unless otherwise specified.)

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $F_{CLKOUT}$ | Low-speed clock output frequency | CLKOUT 250Hz | | 250 | | Hz |
| $F_{CLKOUT;ERR}$ | Low-speed clock output frequency error | $T_A$ = 25°C | -10 | | 10 | % |
| | | $T_A$ = -40°C - 105°C | -15 | | 15 | % |

### Table 11-11 Temperature Protection

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $T_{WARN}$ | Temperature warning threshold | | | 140 | | ºC |
| $T_{WARN;HYS}$ | Temperature warning hysteresis | | | 10 | | ºC |
| $T_{WARN;BLANK}$ | Temperature warning blanking | | | 10 | | µs |
| $T_{FAULT}$ | Temperature fault threshold | | | 165 | | ºC |
| $T_{FAULT;HYS}$ | Temperature fault hysteresis | | | 10 | | ºC |
| $T_{FAULT;BLANK}$ | Temperature fault blanking | | | 10 | | µs |

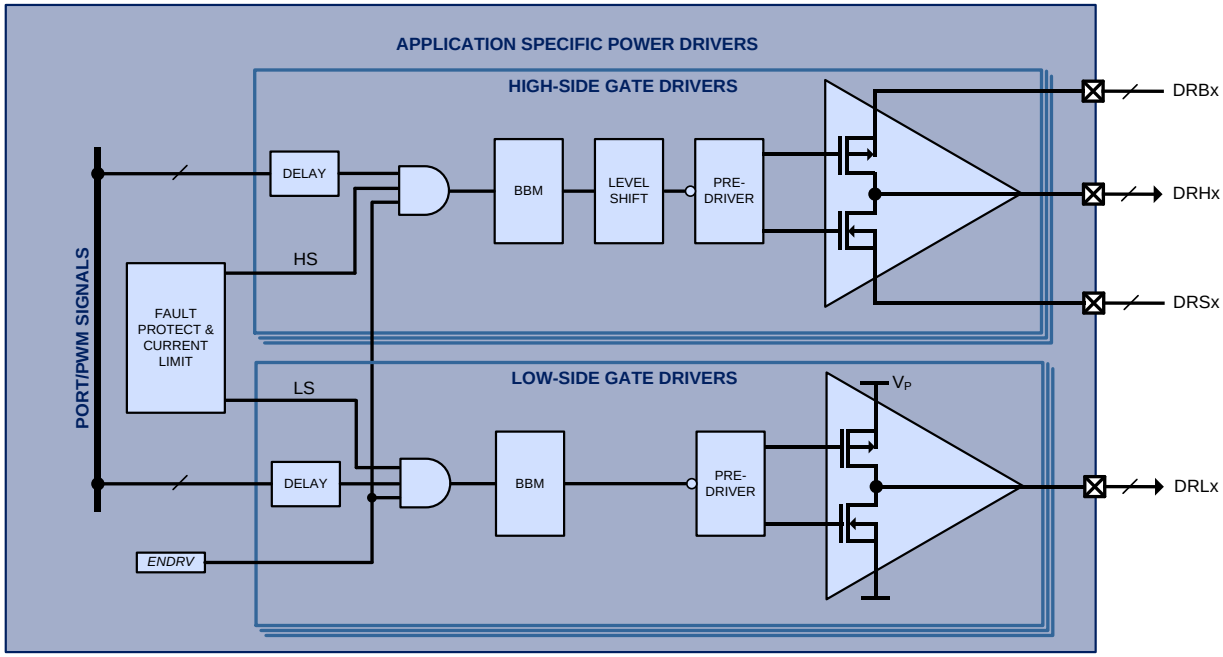
# 12 APPLICATION SPECIFIC POWER DRIVERS (ASPD)

## 12.1 Features

- 3 low-side and 3 high-side gate drivers
- 2A sink/source gate driving capability
- Configurable propagation delays
- Fast fault protection
- Cycle-by-cycle current limit function
- Configurable driver break-before-make (BBM) safety function

## 12.2 Block Diagram

**Figure 12-1 Application Specific Power Drivers**




## 12.3 Functional Description

The Application Specific Power Drivers (ASPD, Figure 12-1) module handles power driving for power and motor control applications. The ASPD contains three low-side gate drivers (DRLx), three high-side gate drivers (DRHx). Each gate driver can drive an external MOSFET or IGBT switch in response to high-speed control signals from the microcontroller ports, and a pair of high-side and low-side gate drivers can form a half-bridge driver.

Figure 12-2 below shows typical gate driver connections and Table 12-1 shows the ASPD available resources. The ASPD gate drivers support up to a 180V source supply.

**Figure 12-2 Typical Gate Driver Connections**

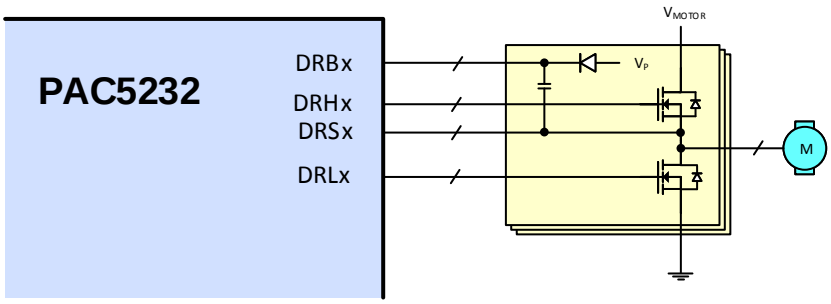



**Table 12-1 Power Driver Resources by Part Numbers**

| PART NUMBER | LOW-SIDE GATE DRIVER | | HIGH-SIDE GATE DRIVER | | |
|---|---|---|---|---|---|
| | DRLx | SOURCE/SINK CURRENT | DRHx | SOURCE/BOOTSTRAP SUPPLY | SOURCE/SINK CURRENT |
| PAC5232 | 3 | 2A/2A | 3 | 165V/180V | 2A/2A |

The ASPD includes built-in configurable fault protection for the internal gate drivers.

## 12.4 Low-Side Gate Driver

The DRLx low-side gate driver drives the gate of an external MOSFET or IGBT switch between the low-level power ground rail and high-level $V_P$ supply rail. The DRLx output pin has sink and source output current capability of 2A. Each low-side gate driver is controlled by a microcontroller port signal with 4 configurable levels of propagation delay.

## 12.5 High-Side Gate Driver

The DRHx high-side gate driver drives the gate of an external MOSFET or IGBT switch between its low-level DRSx driver source rail and its high-level DRBx bootstrap rail. The DRSx pin can go up to 160V steady state (VM + 15V maximum). The DRHx output pin has sink and source output current capability of 2A.

The DRBx bootstrap pin can have a maximum operating voltage of 15V relative to the DRSx pin, and up to 175V steady state. The DRSx pin can have a maximum operating voltage of 10V relative to the VM pin. The DRSx pin is designed to tolerate momentary switching negative spikes down to -10V without affecting the DRHx output state. Each high-side gate driver is controlled by a microcontroller port signal with 4 configurable levels of propagation delay.

For bootstrapped high-side operation, connect an appropriate capacitor between DRBx and DRSx and a properly rated bootstrap diode from $V_P$ to DRBx. To operate the DRHx output as a low-side gate driver, connect its DRBx pin to $V_P$ and its DRSx pin to $V_{SS}$.

## 12.6 Power Drivers Control

All power drivers are initially disabled from power-on-reset. To enable the power drivers, the MCU must first enable the ASPD block. The gate drivers are controlled by the microcontroller ports and/or PWM

signals according to Table 12-2, with configurable delays as shown in Table 12-3 Power Driver Propagation Delay.

Refer to the PAC5232 User Guide and PAC® application notes and user guide for additional information on power drivers control programming.

**Table 12-2 Microcontroller Port and PWM to Power Driver Mapping**

| PART NUMBER | DRL0 | DRL1 | DRL2 | DRH3 | DRH4 | DRH5 |
|---|---|---|---|---|---|---|
| PAC5232 | PWMA0 | PWMA1 | PWMA2 | PWMA3/ PWMA4/ PWMB0 | PWMA5/ PWMC0 | PWMA6/ PWMD0 |

**Table 12-3 Power Driver Propagation Delay**

| DRLx | DRHx |
|---|---|
| 135ns | 155ns |

## 12.7 Gate Driver Fault Protection

The ASPD incorporates a configurable fault protection mechanism using protection signal from the Configurable Analog Front End (CAFE), designated as protection event 1 (PR) signal. The DRL0/DRL1/DRL2 drivers are designated as low-side group 1. The DRH3/DRH4/DRH5 gate drivers are designated as high-side group 1. The PR signal from the CAFE can be used to disable low-side group 1, high-side group 1, or both depending on the PR mask bit settings.

## 12.8 Electrical Characteristics

**Table 12-4 Gate Driver Electrical Characteristics**

($V_P$ = 12V, and $T_A$ = -40°C to 105°C unless otherwise specified.)

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **Low-Side Gate Drivers (DRLx pins)** | | | | | | |
| $V_{OH;DRL}$ | High-level output voltage | $I_{DRLx}$ = -50mA | $V_P$-0.3 | | | V |
| $V_{OL;DRL}$ | Low-level output voltage | $I_{DRLx}$ = 50mA | | | 0.3 | V |
| $I_{OHPK;DRL}$ | Output high source current | 10µs pulse | | 2 | | A |
| $I_{OLPK;DRL}$ | Output low sink current | 10µs pulse | | 2 | | A |
| **High-Side Gate Drivers (DRHx, DRBx and DRSx pins)** | | | | | | |
| $V_{DRS}$ | Level-shift driver source voltage range | | -10 | | VM + 10 | V |
| $V_{DRB}$ | Bootstrap pin voltage range | Relative to $V_{DRS}$ | 10 | | 20 | V |
| | | Relative to VSS | | | 175 | V |
| $V_{UVLO;DRB}$ | Bootstrap UVLO threshold | $V_{DRBx}$ rising | 8.5 | | | V |
| | | Hysteresis | | 1 | | V |
| $I_{BS;DRB}$ | Bootstrap supply current | Current from DRBx to DRSx | | 28 | | µA |

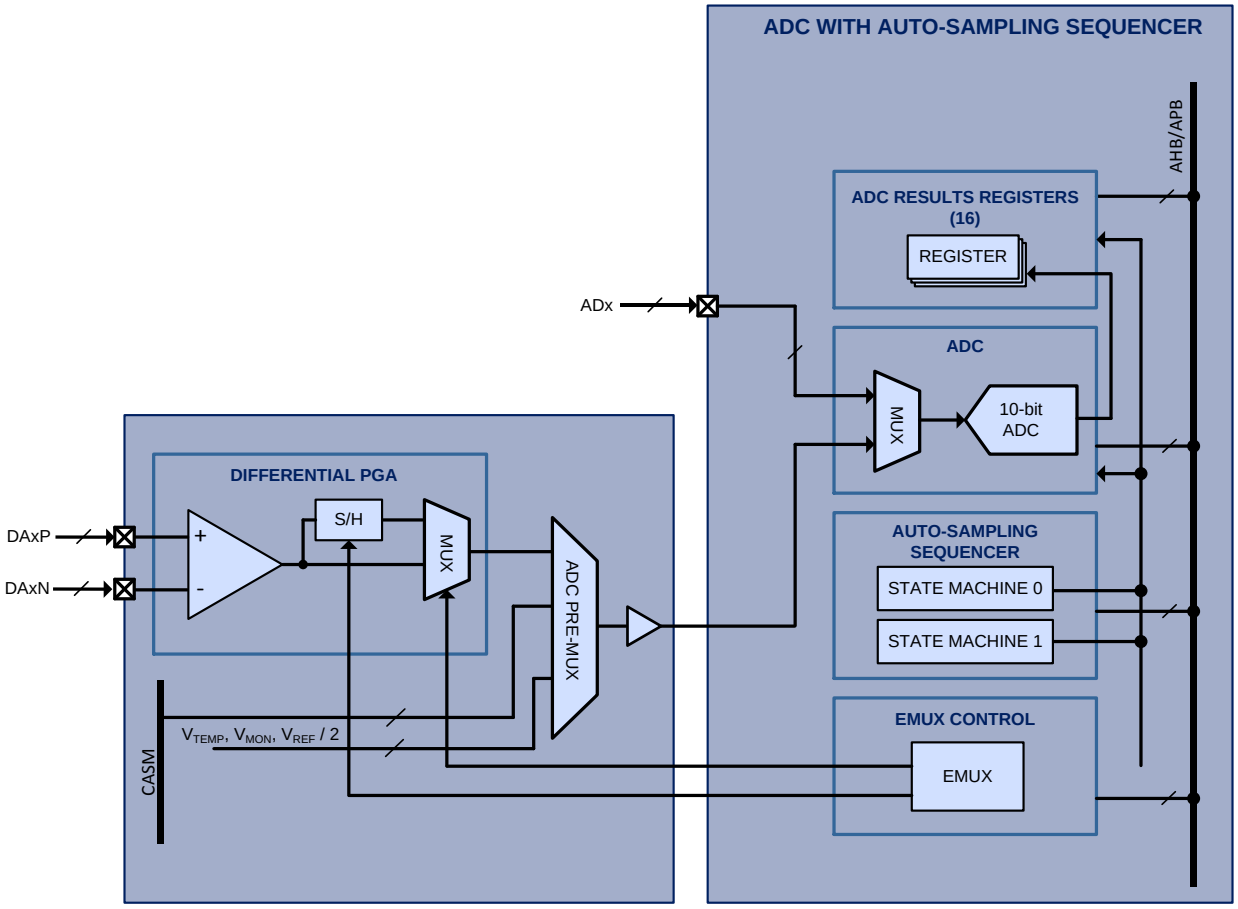
| | | | | | | |
|---|---|---|---|---|---|---|
| $I_{OS;DRB}$ | Offset supply current | Current from DRBx to ground | | 10 | | µA |
| $V_{OH;DRH}$ | High-Level output voltage | $I_{DRHx}$ = -50mA | $V_{DRBx}$-0.3 | | | V |
| $V_{OL;DRH}$ | Low-level output voltage | $I_{DRHx}$ = 50mA | | | $V_{DRSx}$+0.3 | V |
| $I_{OHPK;DRH}$ | Output high source current | 10µs pulse | | 2 | | A |
| $I_{OLPK;DRL}$ | Output low sink current | 10µs pulse | | 2 | | A |
| **High-Side and Low-Side Gate Driver Propagation Delay** | | | | | | |
| $t_{PD}$ | Propagation Delay[5] | Delay setting 00b | -50% | Delay + 0 | 50% | ns |
| | | Delay setting 01b | -50% | Delay + 50 | 50% | ns |
| | | Delay setting 10b | -50% | Delay + 100 | 50% | ns |
| | | Delay setting 11b | -50% | Delay + 200 | 50% | ns |

[5] Delay from Table 12-3 Power Driver Propagation Delay

# 13 ADC WITH AUTO-SAMPLING SEQUENCER

## 13.1 ADC Block Diagram

**Figure 13-1 ADC with Auto-Sampling Sequencer**




## 13.2 Functional Description

### 13.2.1 ADC

The analog-to-digital converter (ADC) is a 10-bit successive approximation register (SAR) ADC with 1 µs conversion time and up to 1MSPS capability. The ADC input clock has a user-configurable divider from /1 to /8 of the system clock. The integrated analog multiplexer allows selection from up to 6 direct ADx inputs, and from up to 10 analog inputs signals in the Configurable Analog Front End (CAFE), including up to 3 differential input pairs. The ADC can be configured for repeating or non-repeating conversions and can interrupt the microcontroller when a conversion is finished.

### 13.2.2 Auto-Sampling Sequencer

Two independent and flexible auto-sampling sequencer state machines allow signal sampling using the ADC without interaction from MCU. Each auto-sampling sequencer state machine can be programmed to take and store up to 8 samples each in the ADC result registers from different analog inputs, is able to control the ADC MUX and ADC Pre-mux as well as the precise timing of the S/H in the Configurable

Analog Front-End (CAFE). The sampling start of the auto-sampling sequencer can be precisely triggered using timers A, B, C, or D or any of their associated PWM edges (high-to-low or low-to-high). It also supports manual start or a ping-pong-scheme, where one auto-sampling sequencer state machine triggers the other when it finishes sampling.

The auto-sampling sequencer can interrupt the microcontroller when either conversion sequence is finished.

### 13.2.3 EMUX Control

A dedicated low latency interface controllable by the auto-sampling sequencer or register control allows changing the ADC pre-multiplexer and asserting/de-asserting the S/H circuit in the Configurable Analog Front-End (CAFE), allowing back to back conversions of multiple analog inputs without MCU interaction.

For more information on the ADC and Auto-Sequencer, see the PAC5232 User Guide.

## 13.3 Electrical Characteristics

### Table 13-1 ADC and Sequencer Electrical Characteristics

($V_{CCIO}$ = 5V and $T_A$ = -40°C to 105°C unless otherwise specified.)

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **ADC** | | | | | | |
| $f_{ADCCLK}$ | ADC conversion clock input | | | | 16 | MHz |
| $f_{ADCCONV}$ | ADC conversion time | $f_{ADCCLK}$ = 16MHz | | | 1 | µs |
| | ADC resolution | | | 10 | | bits |
| | ADC effective resolution | | 9.2 | | | bits |
| | ADC differential non-linearity (DNL) | | | ±0.5 | | LSB |
| | ADC integral non-linearity (INL) | | | ±1 | | LSB |
| | ADC offset error | | | 0.6 | | %FS |
| | ADC gain error | | | 0.12 | | %FS |
| **REFERENCE VOLTAGE** | | | | | | |
| $V_{REFADC}$ | ADC reference voltage input | $V_{REF}$ = 2.5V | | 2.5 | | V |
| | ADC reference voltage input error | $T_A$ = 25ºC | -0.5 | | 0.5 | % |
| **SAMPLE AND HOLD** | | | | | | |
| $t_{ADCSH}$ | ADC sample and hold time | $f_{ADCCLK}$ = 16MHz | | 188 | | µs |
| $C_{ADCIC}$ | ADC input capacitance | ADC MUX input | | 1.3 | | pF |
| **INPUT VOLTAGE RANGE** | | | | | | |
| $V_{ADCIN}$ | ADC input voltage range | ADC MUX input | 0 | | $V_{REFADC}$ | V |
| **EMUX CLOCK SPEED** | | | | | | |
| $f_{EMUXCLK}$ | EMUX engine clock input | | | | 50 | MHz |

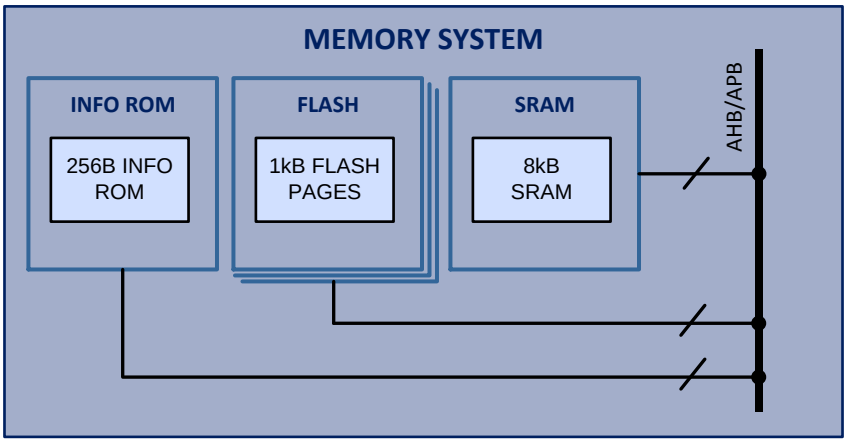
# 14 MEMORY SYSTEM

## 14.1 Features

- 32kB Embedded FLASH
  - 100,000 program/erase cycles
  - 10 years data retention
- 256B INFO Embedded FLASH
  - Device ID, calibration data
  -
- 8kB SRAM
  - 50MHz read/write
  - Data storage or code execution
- SWD code protection

## 14.2 Memory System Block Diagram

**Figure 14-1 Memory System**




## 14.3 Functional Description

The PAC5232 has multiple banks of embedded FLASH memory, SRAM memory as well as peripheral control registers that are program-accessible in a flat memory map.

## 14.4 Program FLASH

The PAC5232 Memory Controller provides access to 32 1kB pages of main program FLASH for a total of 32kB of FLASH through the system AHB bus. Each page may be individually erased or written while the MCU is executing instructions from SRAM.

## 14.5 INFO FLASH

The PAC5232 Memory Controller contains a 256B read-only INFO memory. This memory contains device-specific information such as the device ID and calibration data for the device.

## 14.6 SRAM

The PAC5232 Memory Controller provides access to the 8kB SRAM for non-persistent data storage. The SRAM memory supports word (4B), half-word (2B) and byte addresses with aligned access.

The PAC5232 Memory Controller can read or write data from RAM up to 50MHz. This can be a benefit for time-critical applications. This memory can also be used for program execution when modifying the contents of FLASH.

For more information on the PAC5232 Memory Controller, see the PAC5232 User Guide.

## 14.7 SWD Protection

The PAC5232 allows the user to blow a fuse that prohibits use of the SWD serial interface.

This will prevent unauthorized users from accessing the contents of the device after customer production.

## 14.8 Electrical Characteristics

### Table 14-1 Memory System Electrical Characteristics

($V_{CCIO}$ = 5V, $T_A$ = -40°C to 105°C unless otherwise specified.)

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **Embedded FLASH** | | | | | | |
| $t_{READ;FLASH}$ | FLASH read time | | 40 | | | ns |
| $t_{WRITE;FLASH}$ | FLASH write time | | 20 | | | µs |
| $t_{PERASE;FLASH}$ | FLASH page erase time | | | | 10 | ms |
| $N_{PERASE;FLASH}$ | FLASH program/erase cycles | | | 100k | | cycles |
| $t_{DR;FLASH}$ | FLASH data retention | | 10 | | | years |
| **SRAM** | | | | | | |
| $t_{ACC;SRAM}$ | SRAM access time | Word (32-bits), aligned | 20 | | | ns |

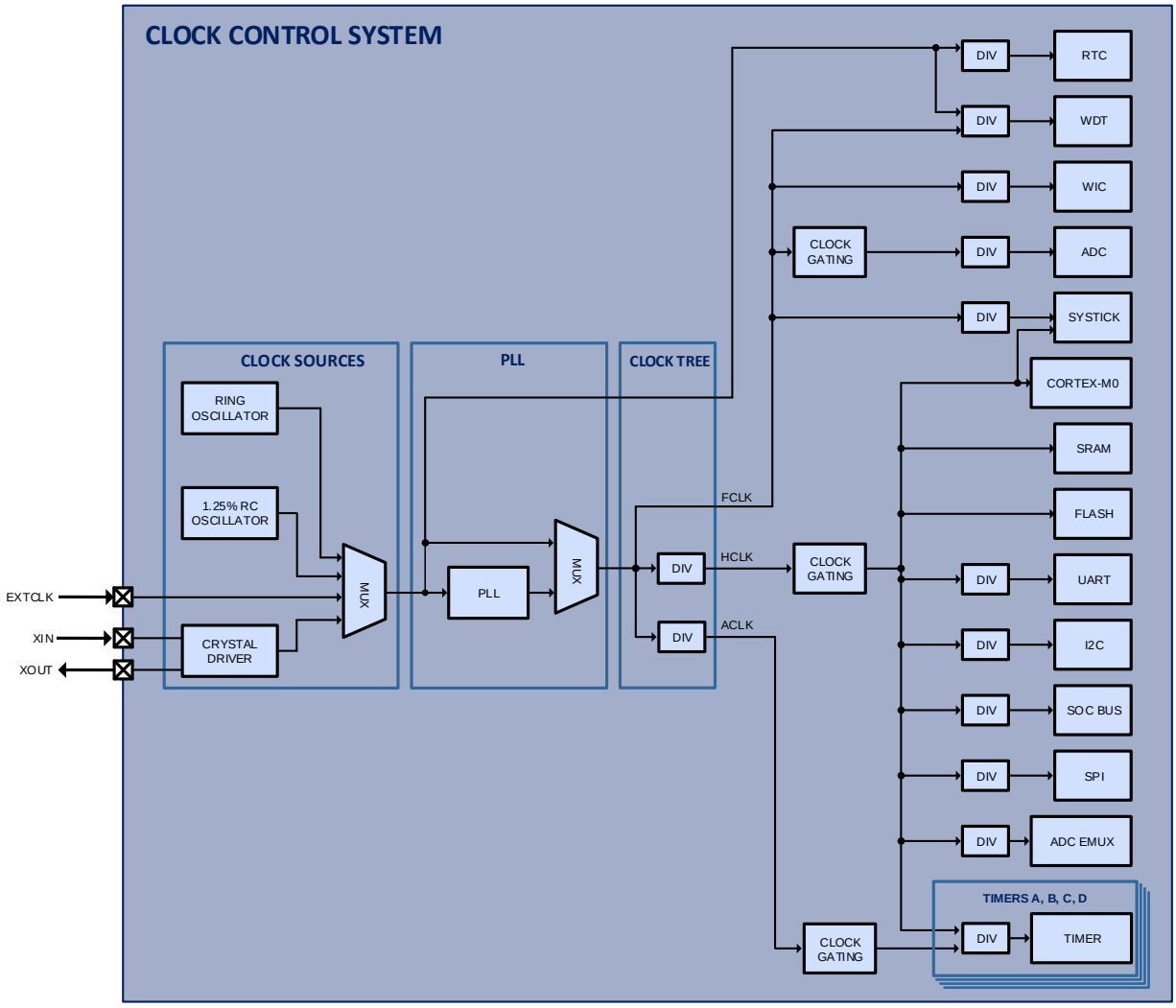
# 15 SYSTEM AND CLOCK CONTROL

## 15.1 Features

- Ring oscillator with 7.5MHz, 9.6MHz, 13.8MHz, and 25.7MHz settings
- High accuracy 1.25% trimmed 4MHz RC oscillator
- External clock input up to 40MHz
- PLL with 1MHz to 25 MHz input, and 3.5MHz to 100MHz output
- /1 to /8 clock divider for HCLK
- /1 to /128 clock divider for ACLK

## 15.2 Block Diagram

**Figure 15-1 Clock Control System**



## 15.3 Functional Description

### 15.3.1 Free-Running Clock (FRCLK)

The free running clock (FRCLK) is generated from one of the 4 clock sources: ring oscillator, trimmed RC oscillator, crystal driver or external clock input. The FRCLK is used for the real-time clock (RTC), watchdog timer (WDT), input to the PLL, or FCLK source to clock the system in low power and sleep mode.

### 15.3.2 Auxiliary Clock (ACLK)

The auxiliary clock (ACLK) is derived from FCLK with a /1, /2, to /128 divider, and supplies the timer and dead-time blocks. It can be clocked faster or slower than HCLK and can go as high as 100MHz.

### 15.3.3 Clock Gating

The clock tree supports clock gating in deep-sleep mode for the timer block, ADC, SPI interface, $I^2C$ interface, UART interface, memory subsystem and the ARM Cortex®-M0 itself.

### 15.3.4 Ring Oscillator (ROSC)

The integrated ring oscillator provides 4 different clocks with 7.5MHz, 9.6MHz, 13.8MHz, and 25.7MHz settings. After reset, the clock tree always defaults to this clock input with the lowest frequency setting.

### 15.3.5 Trimmed 4MHz RC Oscillator

The 1.25% trimmed 4MHz RC oscillator provides an accurate clock suitable for many applications. It is also used to derive the clock for the Multi-Mode Power Manager.

### 15.3.6 External Clock Input

The clock tree can be supplied with an external clock up to 40MHz.

### 15.3.7 PLL

The integrated PLL input clock is supplied by the FRCLK with an input frequency range of 1MHz to 25MHz. The PLL output frequency is adjustable from 3.5MHz to 100MHz.

## 15.4 Electrical Characteristics

### Table 15-1 CCS Electrical Characteristics

($T_A$ = -40°C to 105°C unless otherwise specified.)

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **Clock Tree (FRCLK, FCLK, ACLK, and HCLK)** | | | | | | |
| $f_{FRCLK}$ | Free-running clock frequency | | | | 50 | MHz |
| $f_{FCLK}$ | Fast clock frequency | | | | 100 | MHz |
| $f_{ACLK}$ | Auxiliary clock frequency | After divider | | | 100 | MHz |
| $f_{HCLK}$ | System clock frequency | After divider | | | 50 | MHz |
| **Internal Oscillators** | | | | | | |
| $f_{ROSC}$ | Ring oscillator frequency | Frequency setting = 11b | | 7.5 | | MHz |
| | | Frequency setting = 10b | | 9.6 | | |
| | | Frequency setting = 01b | | 13.8 | | |
| | | Frequency setting = 00b | | 25.7 | | |
| $f_{TRIM}$ | Trimmed RC oscillator frequency | $T_A$ = 25°C | 3.96 | 4 | 4.05 | MHz |
| | | $T_A$ = -40°C to 105°C | 3.92 | 4 | 4.08 | MHz |
| | Trimmed RC oscillator clock jitter | $T_A$ = -40°C to 105°C | | 0.5 | | % |
| **External Clock Input (EXTCLK)** | | | | | | |
| $f_{EXTCLK}$ | External Clock Input Frequency | | | | 40 | MHz |
| $t_{HIGH;EXTCLK}$ | External Clock High Time | | 10 | | | ns |
| $t_{LOW;EXTCLK}$ | External Clock Low Time | | 10 | | | ns |
| $V_{IH;EXTCLK}$ | External Clock Input high-level input voltage | | 2.1 | | | V |
| $V_{IL;EXTCLK}$ | External Clock Input low-level input voltage | | | | 0.825 | V |
| **PLL** | | | | | | |
| $f_{INPLL}$ | PLL input frequency range | | 2 | | 25 | MHz |
| $f_{OUTPLL}$ | PLL output frequency range | | 3.5 | | 100 | MHz |
| | PLL setting time | | | 0.5 | | ms |
| | PLL period jitter | RMS | | 30 | | ps |
| | | Peak to peak | | ±150 | | ps |

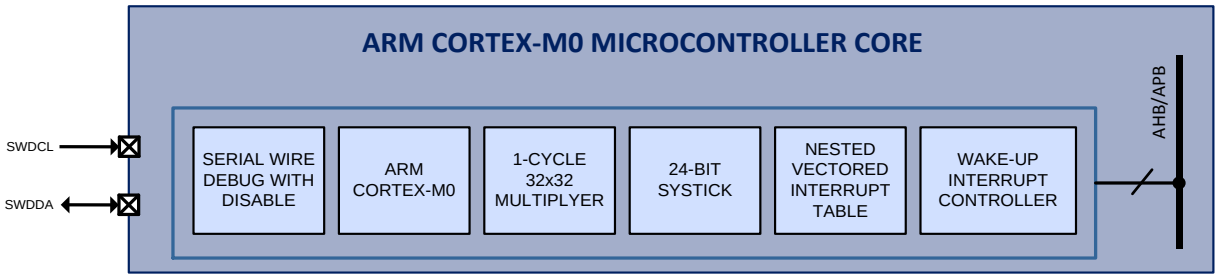
# 16 ARM CORTEX®-M0 MCU CORE

## 16.1 Features

- ARM Cortex®-M0 core
- Fast single-cycle 32-bit x 32-bit multiplier
- 24-bit SysTick timer
- Up to 50MHz operation
- Serial wire debug (SWD), with 4 break-point and 2 watch-point unit comparators
- Nested vectored interrupt controller (NVIC) with 25 external interrupts
- Wake-up interrupt controller (WIC) with GPIO, real-time clock (RTC) and watchdog timer (WDT) interrupts enabled
- Sleep and deep-sleep mode with clock gating

## 16.2 Block Diagram

**Figure 16-1 ARM Cortex®-M0 Microcontroller Core**




## 16.3 Functional Description

The ARM Cortex®-M0 microcontroller core is configured for little endian operation and includes the fast single-cycle 32-bit multiplier and 24-bit SysTick timer and can operate at a frequency of up to 50MHz.

The microcontroller nested vectored interrupt controller (NVIC) supports 25 external interrupts for the device's peripherals and sub-systems. For low-latency interrupt processing, the NVIC also supports interrupt tail-chaining. The wake-up interrupt controller (WIC) is able to wake up the device from low-power modes using any GPIO interrupt, as well as from the RTC or WDT. The ARM Cortex®-M0 supports both sleep and deep-sleep low-power modes. The deep-sleep mode supports clock gating to limit standby power even further.

Firmware debug support includes 4 break-point and 2 watch-point unit comparators using the serial wire debug (SWD) protocol. The serial wire debug mechanism can be disabled to prevent device access to the firmware in the field.

For more information on the detailed operation of the Microcontroller Core in the PAC5232, see the PAC5232 User Guide.

## 16.4 Electrical Characteristics

### Table 16-1 MCU and Clock Control System Electrical Characteristics

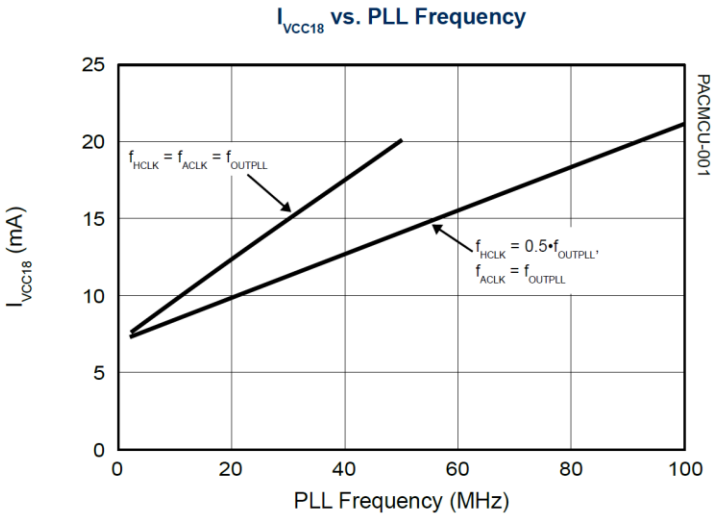
($T_A$ = -40°C to 105°C unless otherwise specified.)

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $f_{HCLK}$ | Microcontroller Clock | HCLK | | | 50 | MHz |
| $I_{OP;VSYS}$ | $V_{SYS}$ operating supply current | $f_{FRCLK}$ = $f_{HCLK}$ = $f_{ACLK}$ = ROSC 11b, PLL disabled, CPU halt; other clock sources, ADC, timers, and serial interfaces disabled | | 3.4 | | mA |
| | | $f_{FRCLK}$ = $f_{HCLK}$ = $f_{ACLK}$ = ROSC 10b, PLL disabled, CPU halt; other clock sources, ADC, timers, and serial interfaces disabled | | 4 | | |
| | | $f_{FRCLK}$ = $f_{HCLK}$ = $f_{ACLK}$ = ROSC 01b, PLL disabled, CPU halt; other clock sources, ADC, timers, and serial interfaces disabled | | 5.3 | | |
| | | $f_{FRCLK}$ = $f_{HCLK}$ = $f_{ACLK}$ = ROSC 00b, PLL disabled, CPU halt; other clock sources, ADC, timers, and serial interfaces disabled | | 9 | | |
| | | $f_{FRCLK}$ = $f_{HCLK}$ = $f_{ACLK}$ = CLKREF, PLL disabled, CPU halt; other clock sources, ADC, timers, and serial interfaces disabled | | 2.3 | | |
| | | $f_{FRCLK}$ = $f_{HCLK}$ = $f_{ACLK}$ = 10MHz XTAL, PLL disabled, CPU halt; other clock sources, ADC, timers, and serial interfaces disabled | | 4.5 | | |
| | | $f_{FRCLK}$ = 4MHz CLKREF, $f_{HCLK}$ = 50MHz, $f_{ACLK}$ = $f_{OUTPLL}$ = 100MHz, CPU halt; other clock sources, ADC, timers, and serial interfaces disabled | | 23.3 | | |
| $I_{Q;VCCIO}$ | $V_{CCIO}$ quiescent supply current | | | 0.02 | | mA |

## 16.5 Typical Performance Characteristics

($V_{SYS}$ = $V_{CCIO}$ = 5V, $T_A$ = -40°C to 105°C unless otherwise specified.)

### Figure 16-2 MCU Performance Characteristics



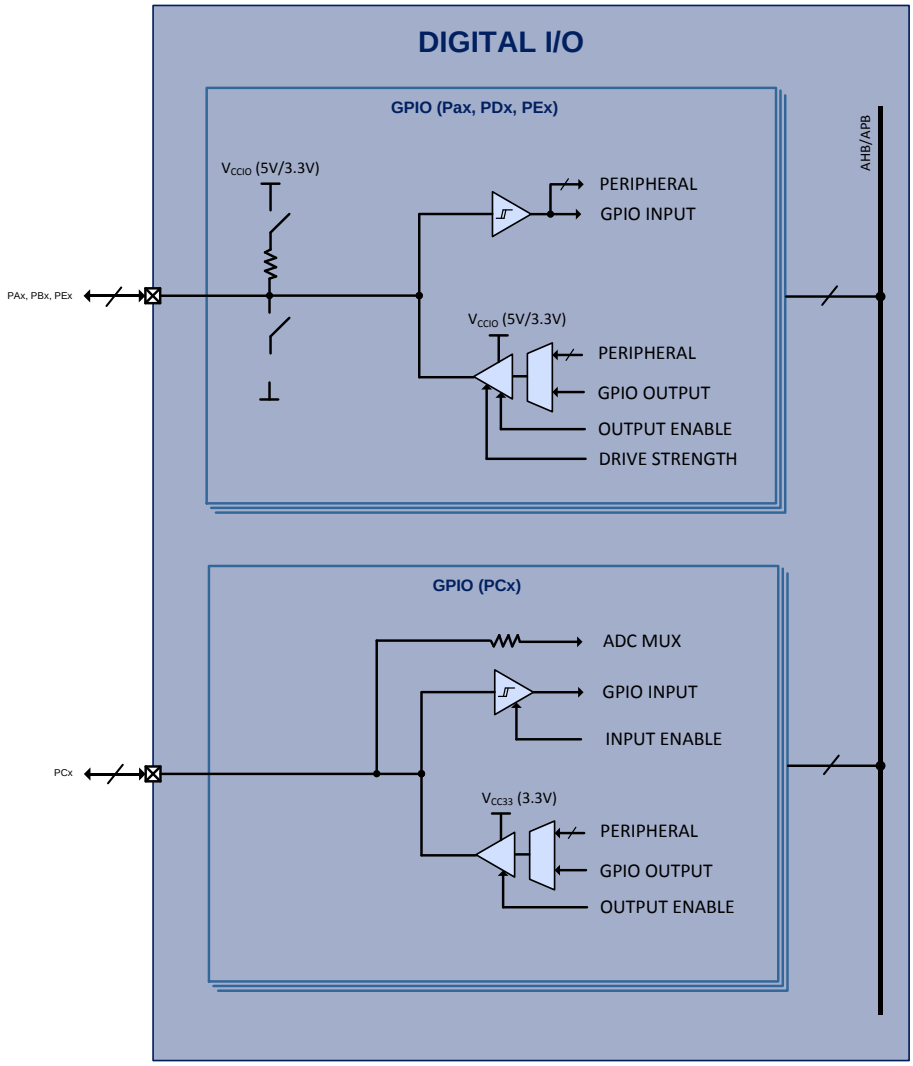
# 17 IO CONTROLLER

## 17.1 Features

- 5V-compliant I/O PAx, PDx, PEx
- 3.3V-compliant I/O PCx
- Configurable drive strength on PAx, PDx, PEx
- Configurable pull-up or pull-down on PAx, PDx, PEx

## 17.2 Block Diagram

**Figure 17-1 IO Controller Block Diagram**



## 17.3 Functional Description

The PAC® can support up to 4 ports with 8 I/Os each from PAx, PCx, PDx, and PEx, in addition to the I/Os on the analog front end. All PAx, PCx, PDx, and PEx ports have interrupt capability with configurable interrupt edge.

PAx, PDx, and PEx I/Os use $V_{CCIO}$ as the I/O supply voltage that is set to 3.3V. To drive these IOs t 5V, the user may short VCCIO and VSYS on the PCB, then 5V will be the supply for these IOs.

The drive current can be configured as 8mA or 16mA. They also support weak pull-up and pull-down to save external components.

PCx uses $V_{CC33}$ as its I/O supply voltage. The drive current is fixed to 8mA. PC0 to PC5 are also associated with analog inputs AD0 to AD5 to the ADC.

## 17.4 Electrical Characteristics

### Table 17-1 IO Controller Electrical Characteristics

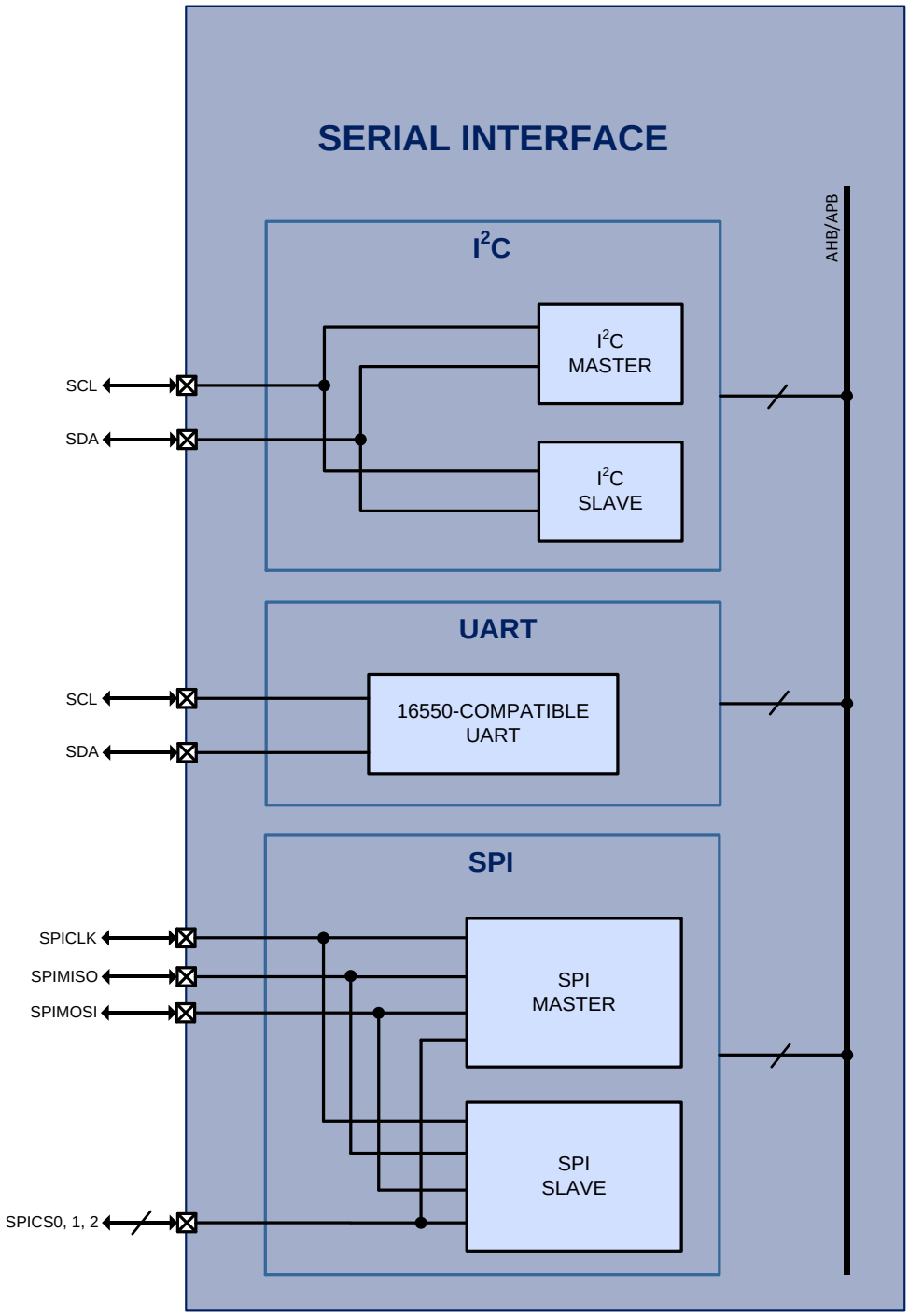
($V_{SYS}$ = $V_{CCIO}$ = 5V, and $T_A$ = -40°C to 105°C unless otherwise specified.)

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| PAx, PDx, PEx (5V Operation) | | | | | | | |
| $V_{IH}$ | High-level input voltage | | | 3 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | | 0.8 | V |
| $I_{OL}$ | Low-level output sink current (Limited by $I_{VSYS}$) | $V_{OL}$ = 0.4V | Drive Strength = 0b | 7 | | | mA |
| | | | Drive Strength = 1b | 15 | | | |
| $I_{OH}$ | High-level output source current (Limited by $I_{VSYS}$) | $V_{OH}$ = 2.4V | Drive Strength = 0b | | | -7 | mA |
| | | | Drive Strength = 1b | | | -15 | |
| $R_{PU}$ | Weak pull-up resistance | $V_{CCIO}$ = 3.3V, pull-up enabled | | 47 | 74 | 104 | kΩ |
| $R_{PD}$ | Weak pull-down resistance | $V_{CCIO}$ = 3.3V, pull-down enabled | | 50 | 84 | 121 | kΩ |
| $I_{IL}$ | Input leakage current | | | -10 | | 10 | µA |
| PCx (3.3V Operation) | | | | | | | |
| $V_{IH}$ | High-level input voltage | $V_{CC33}$ = 3.3V | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | $V_{CC33}$ = 3.3V | | | | 0.8 | V |
| $I_{OL}$ | Low-level output sink current | $V_{CC33}$ = 3.3V, $V_{OL}$ = 0.4V | | 7 | | | mA |
| $I_{OH}$ | High-level output source current | $V_{CC33}$ = 3.3V, $V_{OH}$ = 2.4V | | | | -7 | mA |
| $I_{IL}$ | Input leakage current | $T_A$ = 125°C | | -10 | 0 | 10 | µA |

# 18 SERIAL INTERFACE

## 18.1 Block Diagram

**Figure 18-1 Serial Interface Block Diagram**



## 18.2 Functional Description

The PAC5232 has up to three serial interfaces: $I^2C$, UART and SPI.

## 18.3 $I^2C$ Controller

The $I_2C$ controller is a configurable peripheral that can support various modes of operation:

- $I^2C$ master operation
  - Normal mode (100kHz), fast mode (400kHz), or fast mode plus (1MHz)
  - Single and multi-master
  - Synchronization (multi-master)
  - Arbitration (multi-master)
  - 7-bit or 10-bit slave addressing
- $I^2C$ slave operation
  - Normal mode (100kHz), fast mode (400kHz), or fast mode plus (1MHz)
  - Clock stretching
  - 7-bit or 10-bit slave addressing

The $I_2C$ peripheral may operate either by polling, or can be configured to be interrupt driven for both receive and transmit data.

## 18.4 UART Controller

The UART peripheral is a configurable peripheral that can support various features and modes of operation:

- Programmable clock selection
- National Instruments PC16550D compatible
- 16-deep transmit and receive FIFO and fractional clock divisor
- Up to 3.125Mbps communication speed (with HCLK = 50MHz)

The UART peripheral may operate either by polling, or can be configured to be interrupt driven for both receive and transmit data.

## 18.5 SPI Controller

The device contains an SPI controller that can each be used in either master or slave operation, with the following features:

- SPI master operation
  - Control of up to three different SPI slaves
  - Operation up to 25MHz
  - Flexible multiple transmit mode for variable-size SPI data with user-defined chip-select behavior
  - Chip select “shaping” through programmable additional delay for chip-select setup, hold and wait time
  - for back-to-back transfers
- SPI master or slave operation
  - Supports clock phase and polarity control
  - Data transmission/reception can be on 8-, 16-, 24- or 32-bit boundary

- Selectable data bit ordering (LSB or MSB first)
- Programmable chip select polarity
- Selectable “auto-retransmit” mode

The SPI peripheral may operate either by polling, or can be configured to be interrupt driven for both receive and transmit data.

## 18.6 Dynamic Characteristics

**Table 18-1 Serial Interface Dynamic Characteristics**

($V_{SYS}$ = $V_{CCIO}$ = 5V, and $T_A$ = -40°C to 105°C unless otherwise specified.)

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **I²C** | | | | | | |
| $f_{I2CCLK}$ | I²C input clock frequency | Standard mode (100kHz) | 2.8 | | | MHz |
| | | Full-speed mode (400kHz) | 2.8 | | | MHz |
| | | Fast mode (1MHz) | 6.14 | | | MHz |
| **UART** | | | | | | |
| $f_{UARTCLK}$ | USART input clock frequency | | | | $f_{HCLK}$/16 | MHz |
| | UART baud rate | $f_{HCLK}$ = 50MHz | | | 3.125 | Mbps |
| **SPI** | | | | | | |
| $f_{SPICLK}$ | USART input clock frequency | Master mode | | | $f_{HCLK}$/2 | MHz |
| | | Slave mode | | | $f_{HCLK}$/2 | MHz |

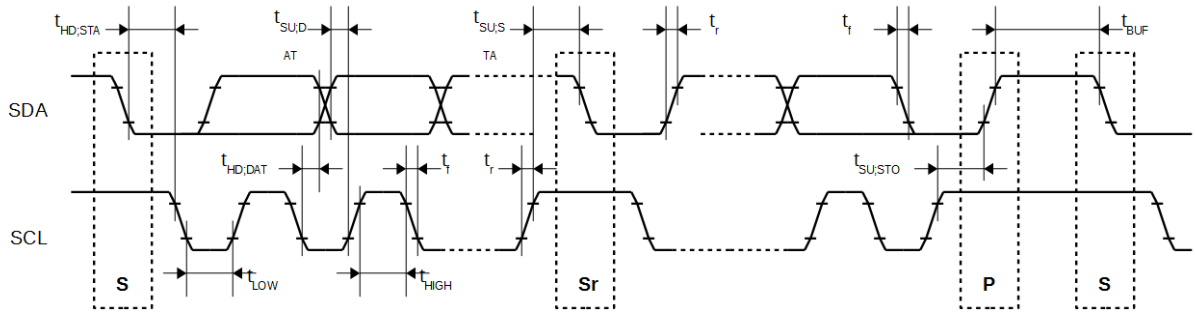
### Table 18-2 I²C Dynamic Characteristics

($V_{SYS}$ = $V_{CCIO}$ = 5V, and $T_A$ = -40°C to 105°C unless otherwise specified.)

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $f_{SCL}$ | SCL clock frequency | Standard mode | 0 | | 100 | kHz |
| | | Full-speed mode | 0 | | 400 | kHz |
| | | Fast mode | 0 | | 1000 | kHz |
| $t_{LOW}$ | SCL clock low | Standard mode | 4.7 | | | µs |
| | | Full-speed mode | 1.3 | | | µs |
| | | Fast mode | 0.5 | | | µs |
| $t_{HIGH}$ | SCL clock high | Standard mode | 4.0 | | | µs |
| | | Full-speed mode | 0.6 | | | µs |
| | | Fast mode | 0.26 | | | µs |
| $t_{HD;STA}$ | Hold time for a repeated START condition | Standard mode | 4.0 | | | µs |
| | | Full-speed mode | 0.6 | | | µs |
| | | Fast mode | 0.26 | | | µs |
| $t_{SU;STA}$ | Set-up time for a repeated START condition | Standard mode | 4.7 | | | µs |
| | | Full-speed mode | 0.6 | | | µs |
| | | Fast mode | 0.26 | | | µs |
| $t_{HD;DAT}$ | Data hold time | Standard mode | 0 | | 3.45 | µs |
| | | Full-speed mode | 0 | | 0.9 | µs |
| | | Fast mode | 0 | | | µs |
| $t_{SU;DAT}$ | Data setup time | Standard mode | 250 | | | ns |
| | | Full-speed mode | 100 | | | ns |
| | | Fast mode | 50 | | | ns |
| $t_{SU;STO}$ | Set-up time for STOP condition | Standard mode | 4.0 | | | µs |
| | | Full-speed mode | 0.6 | | | µs |
| | | Fast mode | 0.26 | | | µs |
| $t_{BUF}$ | Bus free time between a STOP and START condition | Standard mode | 4.7 | | | µs |
| | | Full-speed mode | 1.3 | | | µs |
| | | Fast mode | 0.5 | | | µs |
| $t_r$ | Rise time for SDA and SCL | Standard mode | | | 1000 | ns |
| | | Full-speed mode | 20 | | 300 | ns |
| | | Fast mode | | | 120 | ns |
| $t_f$ | Fall time for SDA and SCL | Standard mode | | | 300 | ns |
| | | Full-speed mode | | | 300 | ns |
| | | Fast mode | | | 120 | ns |

| | | | | | | |
|---|---|---|---|---|---|---|
| $C_b$ | Capacitive load for each bus line | Standard mode, full-speed mode | | | 400 | pF |
| | | Fast mode | | | 550 | pF |

**Figure 18-2 I²C Timing Diagram**

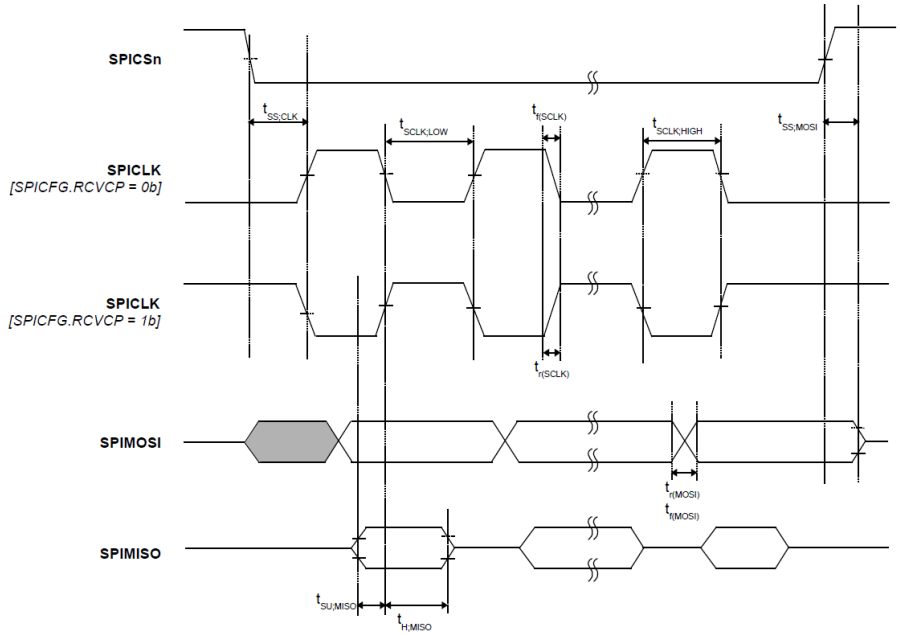


### Table 18-3 SPI Dynamic Characteristics

($V_{SYS}$ = $V_{CCIO}$ = 5V, and $T_A$ = -40°C to 105°C unless otherwise specified.)

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{SCLK;HIGH}$ | SPICLK Input High Time | SPICLK = 25MHz | 30 | | | ns |
| $t_{SCLK;LOW}$ | SPICLK Input low Time | | 30 | | | ns |
| $t_{SS;SCLK}$ | SPICSn to SPICLK Time | | 120 | | | ns |
| $t_{SS;MOSI}$ | SPICSn to SPIMISO High-impedance time | | 10 | | 50 | ns |
| $t_{r(SCLK)}$ | SPICLK Rise Time | | | 10 | 25 | ns |
| $t_{f(SCLK)}$ | SPICLK Fall Time | | | 10 | 25 | ns |
| $t_{r(MOSI)}$ | SPIMOSI Rise Time | | | 10 | 25 | ns |
| $t_{f(MOSI)}$ | SPIMOSI Fall Time | | | 10 | 25 | ns |
| $t_{r(MISO)}$ | SPIMISO Rise Time | | | 10 | 25 | ns |
| $t_{f(MISO)}$ | SPIMISO Fall Time | | | 10 | 25 | ns |
| $t_{SU;MISO}$ | SPIMISO Setup Time | | 20 | | | ns |
| $t_{H;MISO}$ | SPIMISO Hold Time | | 20 | | | ns |

### Figure 18-3 SPI Timing Diagram



# 19 TIMERS

## 19.1 Block Diagram

**Figure 19-1 PWM Timers Block Diagram**

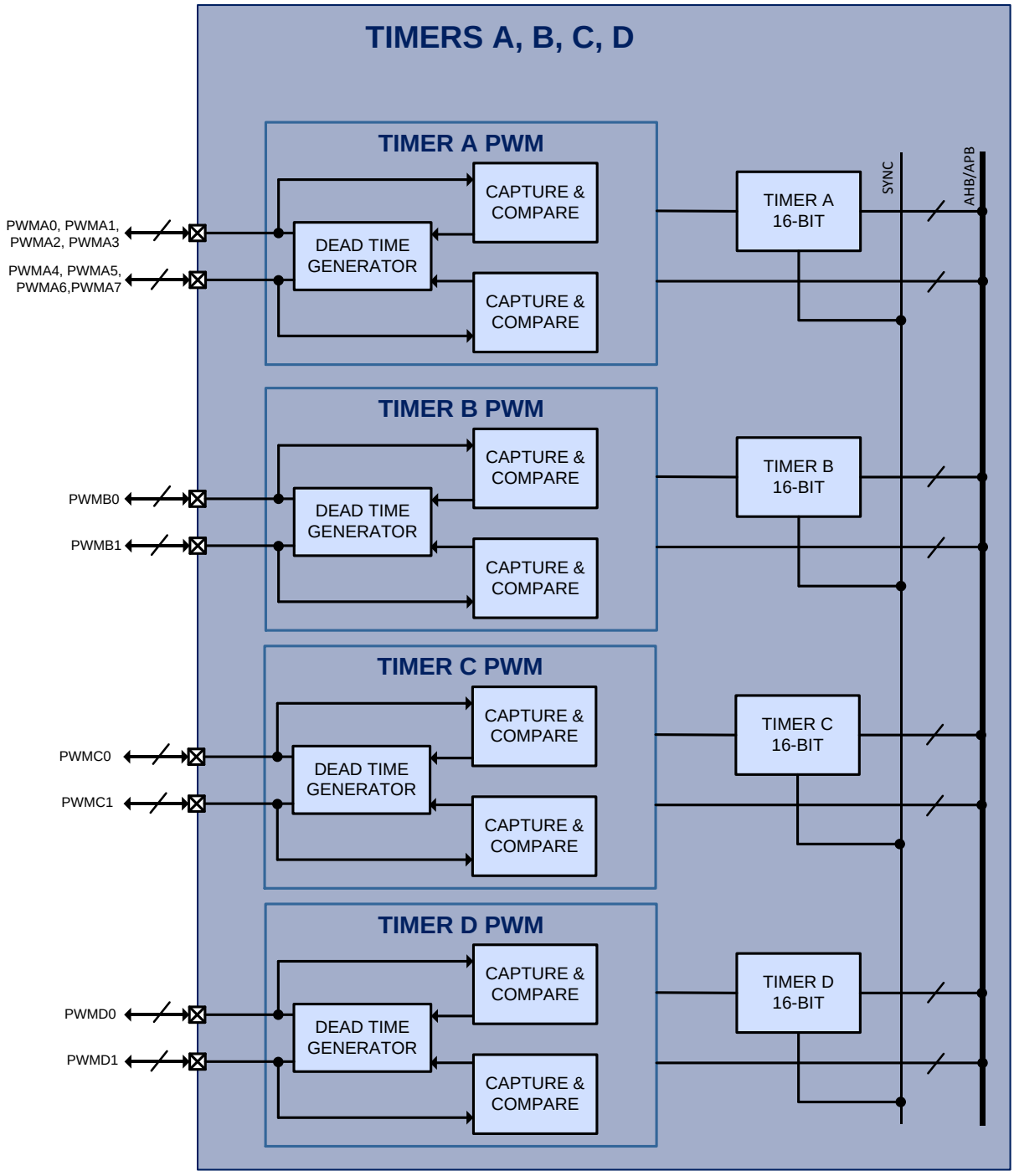


Figure 19-2 SOC Bus Watchdog and Wake-Up Timer

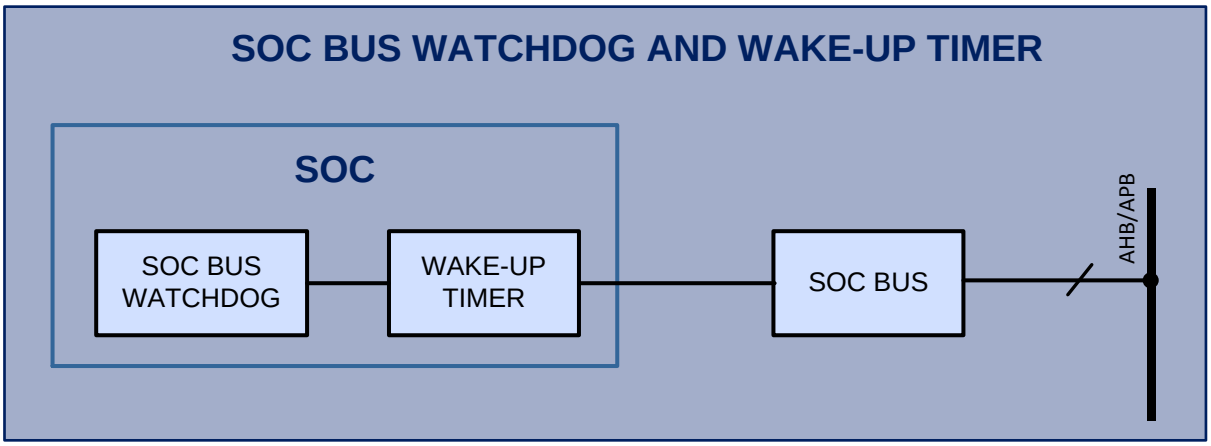
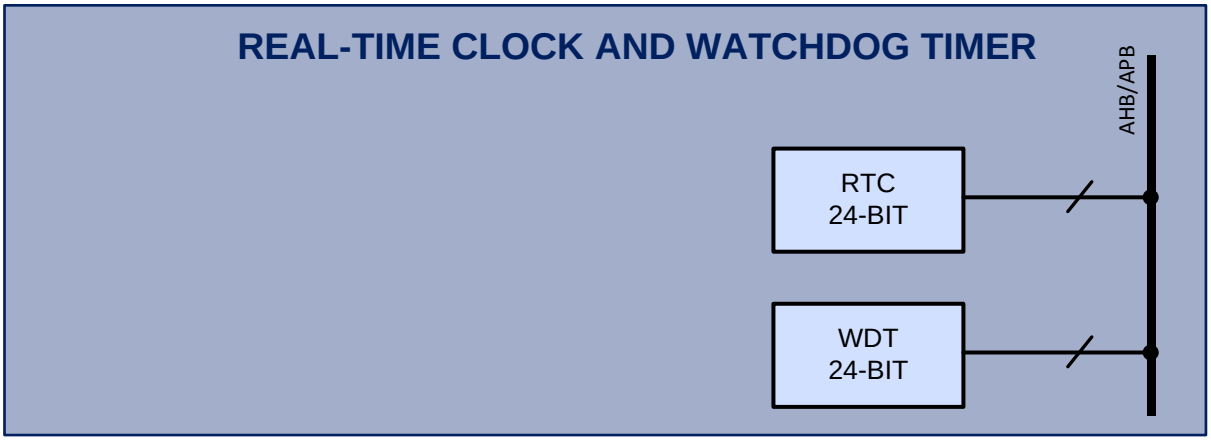



Figure 19-3 Real-Time Clock and Watchdog Timer




## 19.2 Functional Description

The device includes 9 timers: timer A, timer B, timer C, timer D, watchdog timer 1 (WDT), watchdog timer 2, wake-up timer, real-time clock (RTC), and SysTick timer. The device supports up to 14 different PWM signals and has up to 7 dead-time controllers. Timers A, B, C and D can be concatenated to synchronize to a single clock and start/stop signal for applications that require a synchronized timer period between timers.

### 19.2.1 Timer A

Timer A is a general purpose 16-bit timer with 8 PWM/capture and compare units. It has 4 pairs of PWM signals going into 4 dead-time controllers. Timer A can be concatenated with timers B, C, and D to synchronize the PWM/capture and compare units. It can use either ACLK or HCLK as clock input with an additional clock divider from /1 to /128.

### 19.2.2 Timer B

Timer B is a general purpose 16-bit timer with 2 PWM/capture and compare units. It has one pair of PWM signals going into one dead-time controller, as well as 2 additional compare units that can be used for

additional system time bases for interrupts. Timer B can be concatenated with timers A, C, and D to synchronize the PWM/capture and compare units. It can use either ACLK or HCLK as clock input with an additional clock divider from /1 to /128.

### 19.2.3 Timer C

Timer C is a general purpose 16-bit timer with 2 PWM/capture and compare units. It has one pair of PWM signals going into one dead-time controller. Timer C can be concatenated with timers A, B, and D to synchronize the PWM/capture and compare units. It can use either ACLK or HCLK as clock input with an additional clock divider from /1 to /128.

### 19.2.4 Timer D

Timer D is a general purpose 16-bit timer with 2 PWM/capture and compare units. It has one pair of PWM signals going into one dead-time controller. Timer D can be concatenated with timers A, B, and C to synchronize the PWM/capture and compare units. It can use either ACLK or HCLK as clock input with an additional clock divider from /1 to /128.

### 19.2.5 Watchdog Timer

The 24-bit watchdog timer (WDT) can be used for long time period measurements or periodic wake up from sleep mode.

The watchdog timer can be used as a system watchdog, or as an interval timer, or both. The watchdog timer can use either FRCLK or FCLK as clock input with an additional clock divider from /2 to /65536.

### 19.2.6 SOC Bus Watchdog Timer

The watchdog timer 2 is used to monitor internal SOC Bus communication. It will trigger device reset if there is no SOC Bus communication to the AFE for 4s or 8s.

### 19.2.7 Wake-Up Timer

The wake-up timer can be used for very low power hibernate and sleep modes to wake up the micro controller periodically.

It can be configured to be 125ms, 250ms, 500ms, 1s, 2s, 4, or 8s.

### 19.2.8 Real-Time Clock

The 24-bit real-time clock (RTC) can be used for time measurements when an accurate clock source is used. This timer can also be used for periodic wake up from sleep mode. The RTC uses FRCLK as clock input with an additional clock divider from /2 to /65536.

# 20 THERMAL CHARACTERISTICS

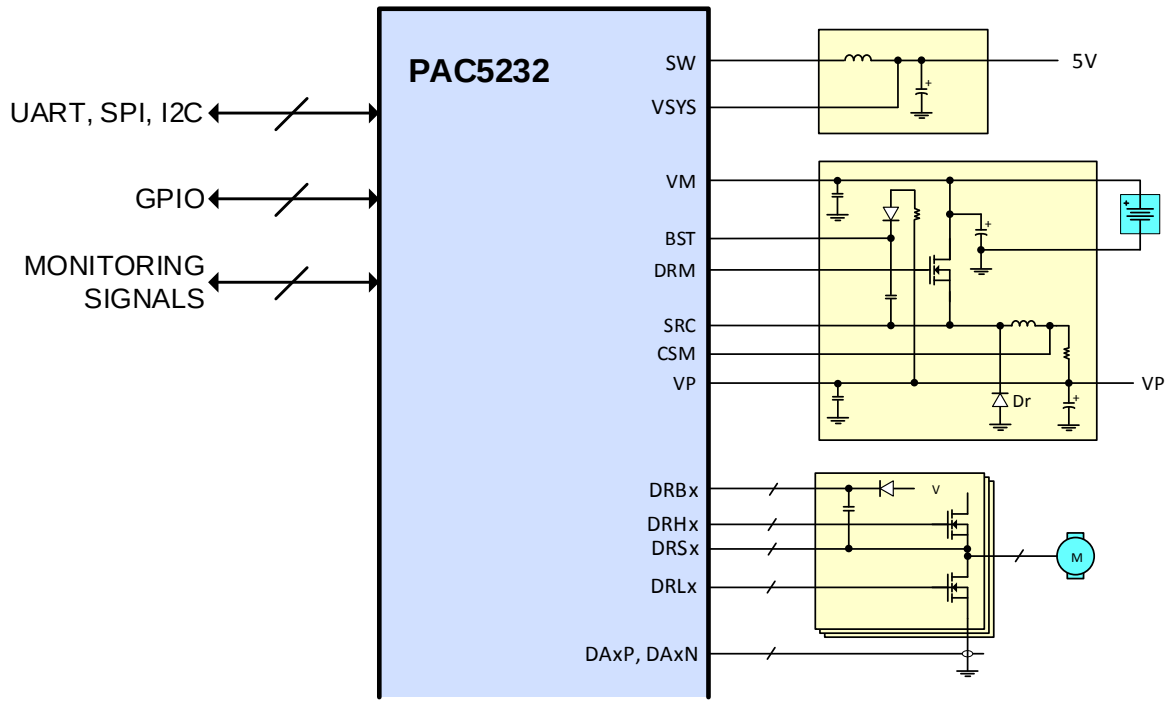
**Table 20-1 Thermal Characteristics**

| PARAMETER | VALUE | UNIT |
|---|---|---|
| Operating ambient temperature range | -40 to 105 | °C |
| Operating junction temperature range | -40 to 125 | °C |
| Storage temperature range | -55 to 150 | °C |
| Lead temperature (Soldering, 10 seconds) | 300 | °C |
| Junction-to-case thermal resistance ($\Theta_{JC}$) | 2.897 | °C/W |
| Junction-to-ambient thermal resistance ($\Theta_{JA}$) | 23.36 | °C/W |

# 21 APPLICATION EXAMPLES

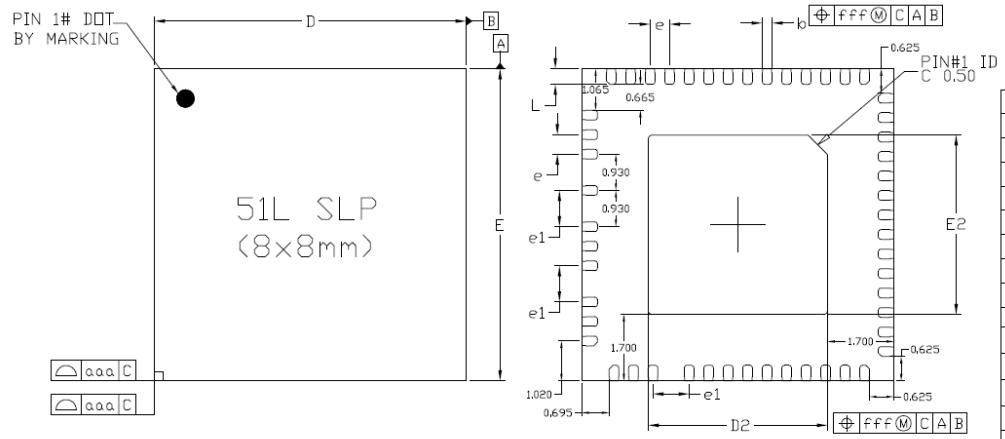
The following simplified diagram shows an example of a single-motor, low-voltage application using the PAC5232 device.

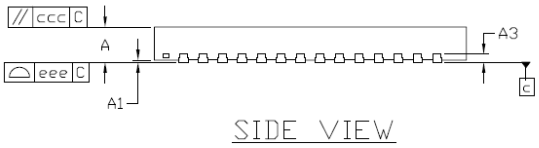
**Figure 21-1 3-Phase Motor Using PAC5232 (Simplified Diagram)**



# 22 PACKAGE OUTLINE AND DIMENSIONS

## 22.1 51L 8x8 QFN Package Outline and Dimensions




Notes

1. All DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER JEDEC MO-220.

| Dimensional Ref. | | | |
|---|---|---|---|
| REF. | Min. | Nom. | Max. |
| A | 0.800 | 0.850 | 0.900 |
| A1 | 0.000 | --- | 0.050 |
| A3 | 0.203 Ref. | | |
| D | 7.950 | 8.000 | 8.050 |
| E | 7.950 | 8.000 | 8.050 |
| D2 | 4.550 | 4.600 | 4.650 |
| E2 | 4.550 | 4.600 | 4.650 |
| | --- | | |
| b | 0.200 | 0.250 | 0.300 |
| L | 0.350 | 0.400 | 0.450 |
| e | 0.500 BSC | | |
| e1 | 0.930 BSC | | |
| Tol. of Form&Position | | | |
| aaa | 0.10 | | |
| bbb | 0.10 | | |
| ccc | 0.10 | | |
| ddd | 0.05 | | |
| eee | 0.08 | | |
| fff | 0.10 | | |

# 23 LEGAL INFORMATION



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