FAIRCHILD
SEMICONDUCTOR®

December 2004

FDM606P

P-Channel 1.8V Logic Level Power Trench® MOSFET

General Description

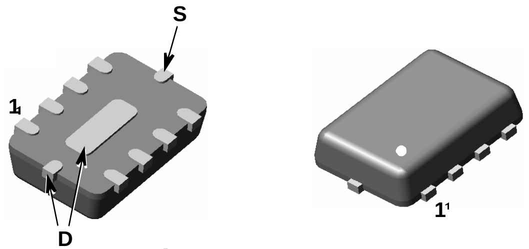
This P-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench process that has been especially tailored to minimize the on-state resistance and yet maintain low gate charge for superior switching performance. These devices are well suited for portable electronics applications.

Applications

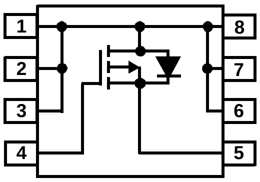
- Load switch
- Battery charge
- Battery disconnect circuits

Features

- Fast switching
- $r_{DS(ON)}$ = 0.026Ω (Typ), V_{GS} = -4.5V
- $r_{DS(ON)}$ = 0.033Ω (Typ), V_{GS} = -2.5V
- $r_{DS(ON)}$ = 0.052Ω (Typ), V_{GS} = -1.8V



MicroFET 3x2-8



MOSFET Maximum Ratings T_A=25°C unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DSS}	Drain to Source Voltage	-20	V
V_{GS}	Gate to Source Voltage	±8	V
I_D	Drain Current		
	Continuous (T_C = 25^{o}C, V_{GS} = - 4.5V)	-6.8	A
	Continuous (T_C = 100^{o}C, V_{GS} = - 2.5V)	-3.8	A
	Continuous (T_C = 100^{o}C, V_{GS} = -1.8V)	-3.0	A
	Pulsed	Figure 4	
P_D	Power dissipation Derate above 25°C	1.92 15.4	W mW/^{o}C
T_J, T_{STG}	Operating and Storage Temperature	-55 to 150	^{o}C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance Junction to Case (Note1)	6.0	^{o}C/W
$R_{\theta JA}$	Thermal Resistance Junction to Ambient (Note 2)	65	^{o}C/W
$R_{\theta JA}$	Thermal Resistance Junction to Ambient (Note 3)	208	^{o}C/W

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
.06P	FDM606P	MicroFET3x2	178 mm	8 mm	3000

Electrical Characteristics T_A = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions		Min	Typ	Max	Units
Off Characteristics							
B_{VDSS}	Drain to Source Breakdown Voltage	I_D = -250µA, V_{GS} = 0V		-20	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = -16V V_{GS} = 0V		-	-	-1	µA
			T_A=100°C	-	-	-5	
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±8V		-	-	±100	nA
On Characteristics							
$V_{GS(TH)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = -250µA		-0.4	-0.9	-1.5	V
$r_{DS(ON)}$	Drain to Source On Resistance	I_D = -6.8A, V_{GS} = -4.5V		-	0.026	0.030	Ω
		I_D = -3.8A, V_{GS} = -2.5V		-	0.033	0.038	
		I_D = -3.0A, V_{GS} = -1.8V		-	0.052	0.070	
Dynamic Characteristics							
C_{ISS}	Input Capacitance	V_{DS} = -10V, V_{GS} = 0V, f = 1MHz		-	2200	-	pF
C_{OSS}	Output Capacitance			-	350	-	pF
C_{RSS}	Reverse Transfer Capacitance			-	160	-	pF
$Q_{g(TOT)}$	Total Gate Charge at -4.5V	V_{GS} = 0V to -4.5V	V_{DD} = -10V I_D = -3.0A I_g = 1.0mA	-	20	30	nC
$Q_{g(-2.5)}$	Total Gate Charge at -2.5V	V_{GS} = 0V to -2.5V		-	12	18	nC
Q_{gs}	Gate to Source Gate Charge			-	3.0	-	nC
Q_{gd}	Gate to Drain “Miller” Charge			-	3.8	-	nC
Switching Characteristics (V_{GS} = -4.5V)							
t_{ON}	Turn-On Time	V_{DD} = -10V, I_D = -3.0A V_{GS} = -4.5V, R_{GS} = 6.8Ω		-	-	81	ns
$t_{d(ON)}$	Turn-On Delay Time			-	9	-	ns
t_r	Rise Time			-	46	-	ns
$t_{d(OFF)}$	Turn-Off Delay Time			-	134	-	ns
t_f	Fall Time			-	71	-	ns
t_{OFF}	Turn-Off Time			-	-	308	ns
Drain-Source Diode Characteristics							
V_{SD}	Source to Drain Diode Voltage	I_{SD} = -6.8A		-	-0.9	-1.2	V
t_{rr}	Reverse Recovery Time	I_{SD} = -3.0A, dI_{SD}/dt = 100A/µs		-	-	28	ns
Q_{RR}	Reverse Recovered Charge	I_{SD} = -3.0A, dI_{SD}/dt = 100A/µs		-	-	20	nC

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the center drain pad. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by user's board design.

2. $R_{\theta JA}$ is 65 ^{o}C/W (steady state) when mounted on a 1 inch^2 copper pad on FR-4.

3. $R_{\theta JA}$ is 208 ^{o}C/W (steady state) when mounted on a minimum pad area.

Typical Characteristic T_A = 25°C unless otherwise noted

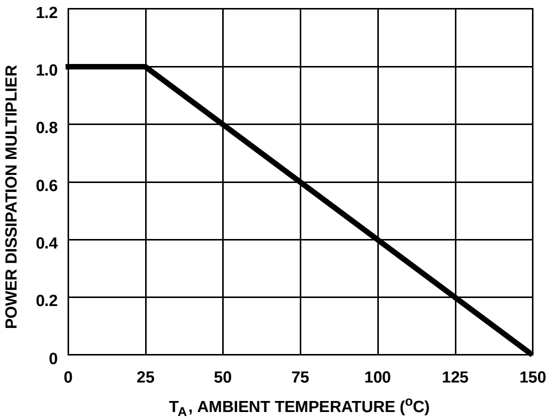


Figure 1. Normalized Power Dissipation vs Ambient Temperature

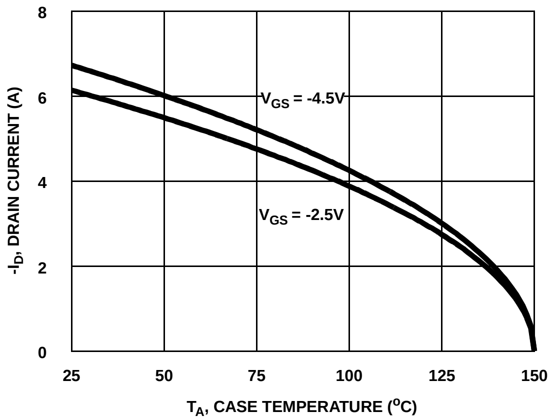


Figure 2. Maximum Continuous Drain Current vs Case Temperature

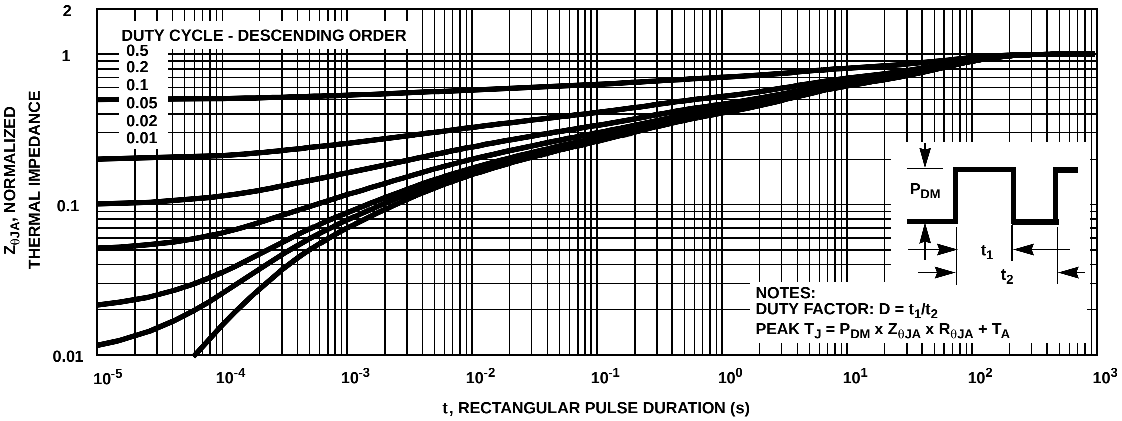


Figure 3. Normalized Maximum Transient Thermal Impedance

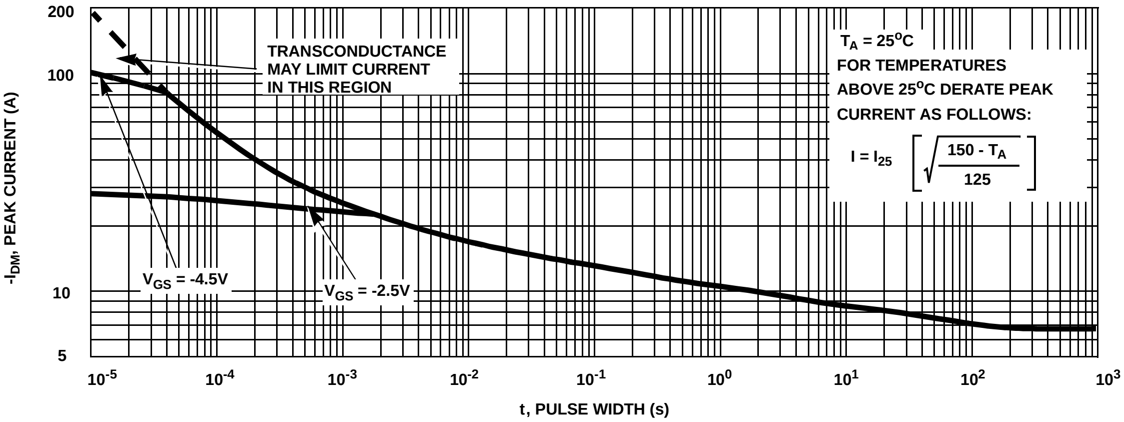


Figure 4. Peak Current Capability

Typical Characteristic (Continued) T_A = 25°C unless otherwise noted

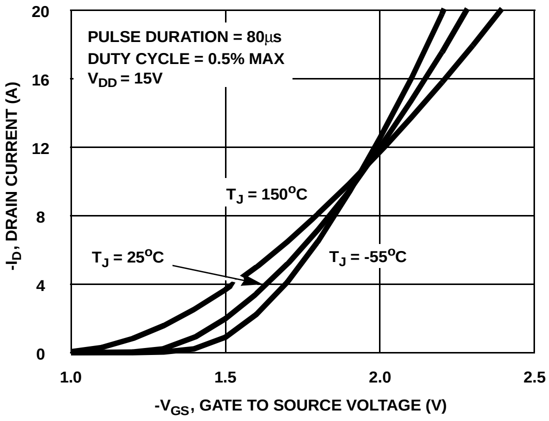


Figure 5. Transfer Characteristics

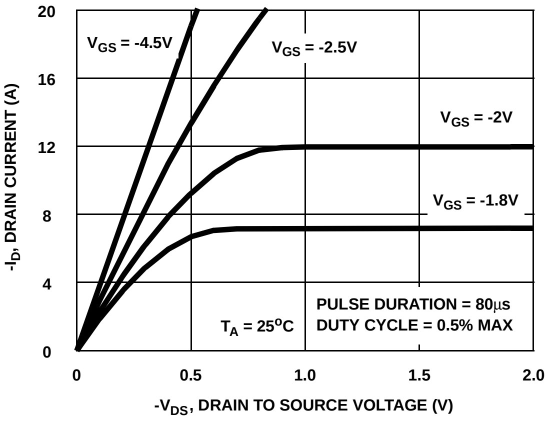


Figure 6. Saturation Characteristics

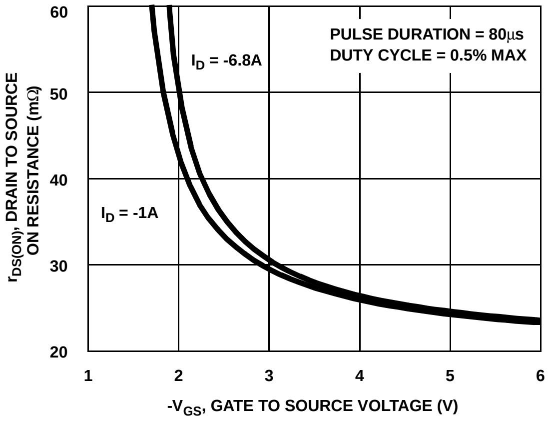


Figure 7. Drain to Source On Resistance vs Gate Voltage and Drain Current

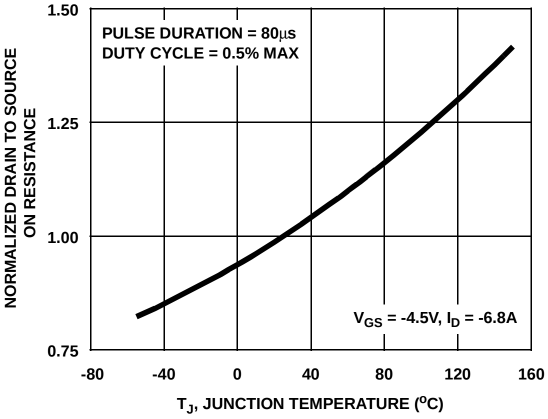


Figure 8. Normalized Drain to Source On Resistance vs Junction Temperature

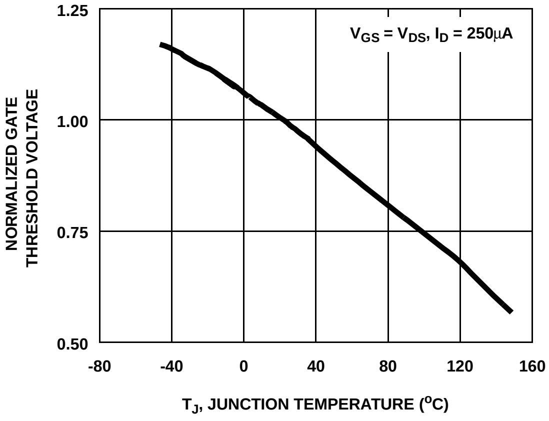


Figure 9. Normalized Gate Threshold Voltage vs Junction Temperature

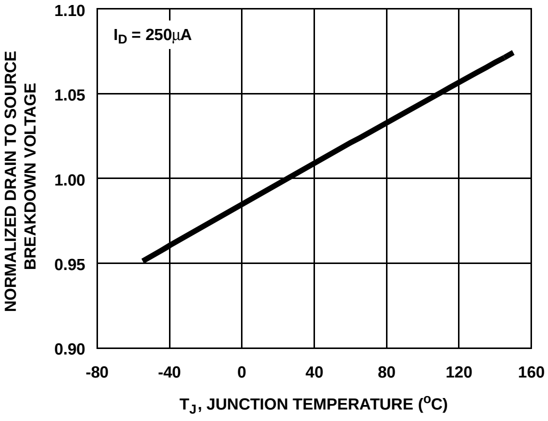


Figure 10. Normalized Drain to Source Breakdown Voltage vs Junction Temperature

Typical Characteristic (Continued) T_A = 25°C unless otherwise noted

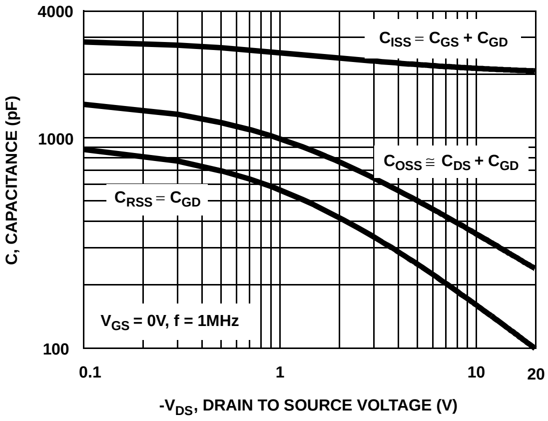


Figure 11. Capacitance vs Drain to Source Voltage

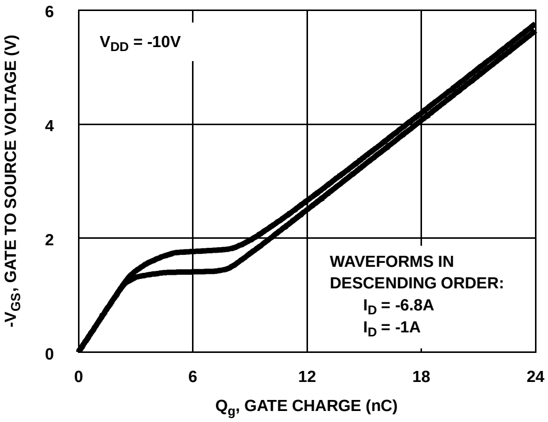


Figure 12. Gate Charge Waveforms for Constant Gate Currents

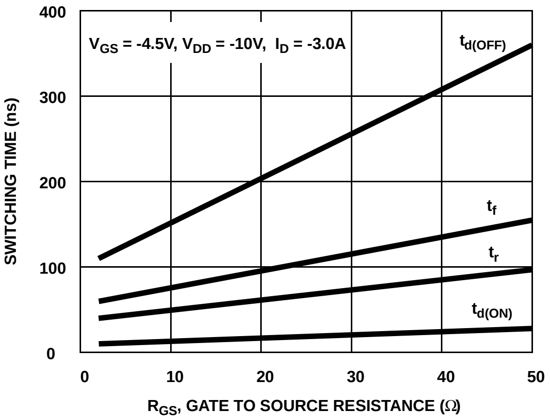


Figure 13. Switching Time vs Gate Resistance

Test Circuits and Waveforms

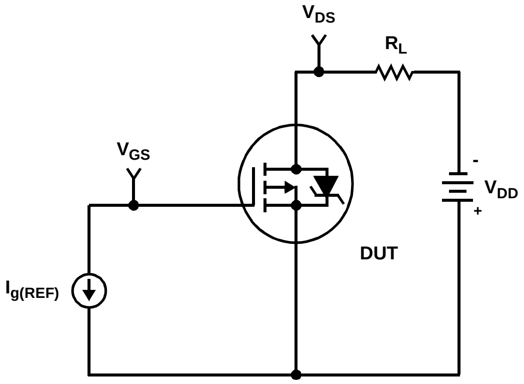


Figure 14. Gate charge Test Circuit

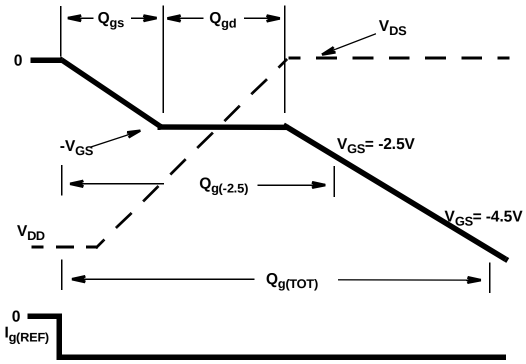


Figure 15. Gate Charge Waveforms

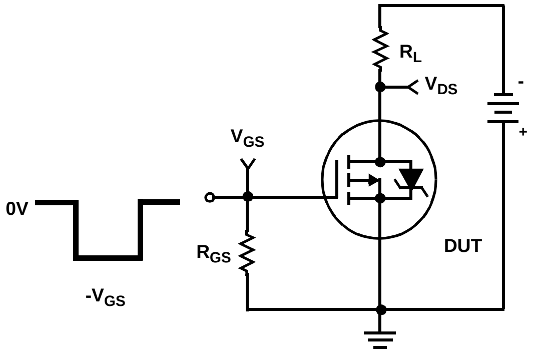


Figure 16. Switching Time Test Circuit

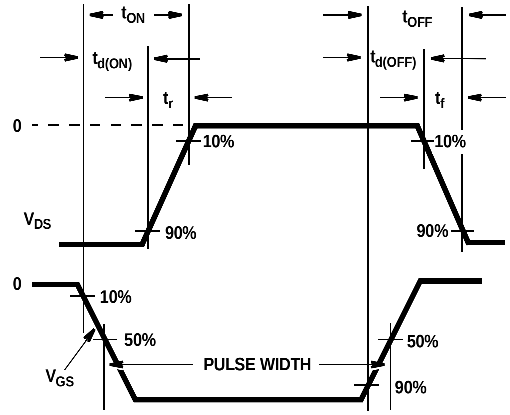


Figure 17. Switching Time Waveforms

Thermal Resistance vs. Mounting Pad Area

The maximum rated junction temperature, T_{JM}, and the thermal resistance of the heat dissipating path determines the maximum allowable device power dissipation, P_{DM}, in an application. Therefore the application's ambient temperature, T_A (^oC), and thermal resistance $R_{\theta JA}$ ($^oC/W$) must be reviewed to ensure that T_{JM} is never exceeded. Equation 1 mathematically represents the relationship and serves as the basis for establishing the rating of the part.

$$P_{DM} = \frac{(T_{JM} - T_A)}{Z_{\theta JA}} \qquad \text{(EQ. 1)}$$

In using surface mount devices such as the MicroFET package, the environment in which it is applied will have a significant influence on the part's current and maximum power dissipation ratings. Precise determination of P_{DM} is complex and influenced by many factors:

1. Mounting pad area onto which the device is attached and whether there is copper on one side or both sides of the board.
2. The number of copper layers and the thickness of the board.
3. The use of external heat sinks.
4. The use of thermal vias.
5. Air flow and board orientation.
6. For non steady state applications, the pulse width, the duty cycle and the transient thermal response of the part, the board and the environment they are in.

Fairchild provides thermal information to assist the designer's preliminary application evaluation. Figure 18 defines the $R_{\theta JA}$ for the device as a function of the top copper (component side) area. This is for a horizontally positioned FR-4 board with 1oz copper after 1000 seconds of steady state power with no air flow. This graph provides the necessary information for calculation of the steady state junction temperature or power dissipation. Pulse applications can be evaluated using the Fairchild device Spice thermal model or manually utilizing the normalized maximum transient thermal impedance curve.

Thermal resistances corresponding to other copper areas can be obtained from Figure 18 or by calculation using Equation 2. The area, in square inches is the top copper area including the gate and source pads.

$$R_{\theta JA} = 58.9 + \frac{6.8}{(0.041 + Area)} \qquad \text{(EQ. 2)}$$

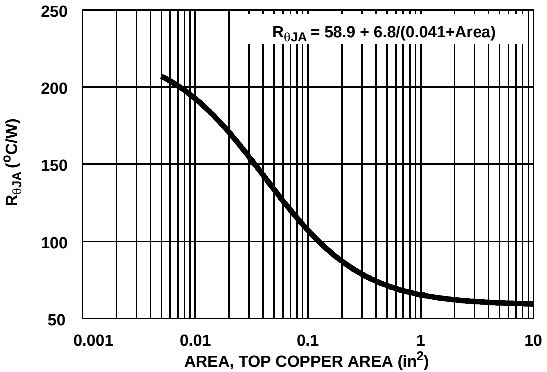
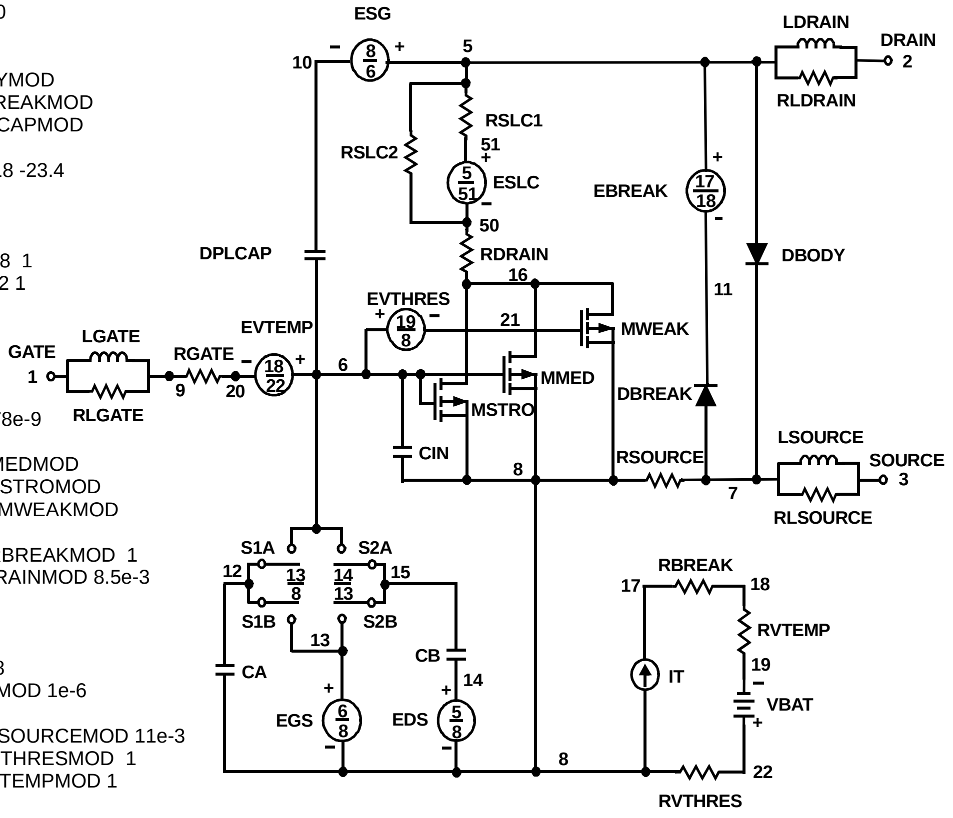


Figure 18. Thermal Resistance vs Mounting Pad Area

PSPICE Electrical Model

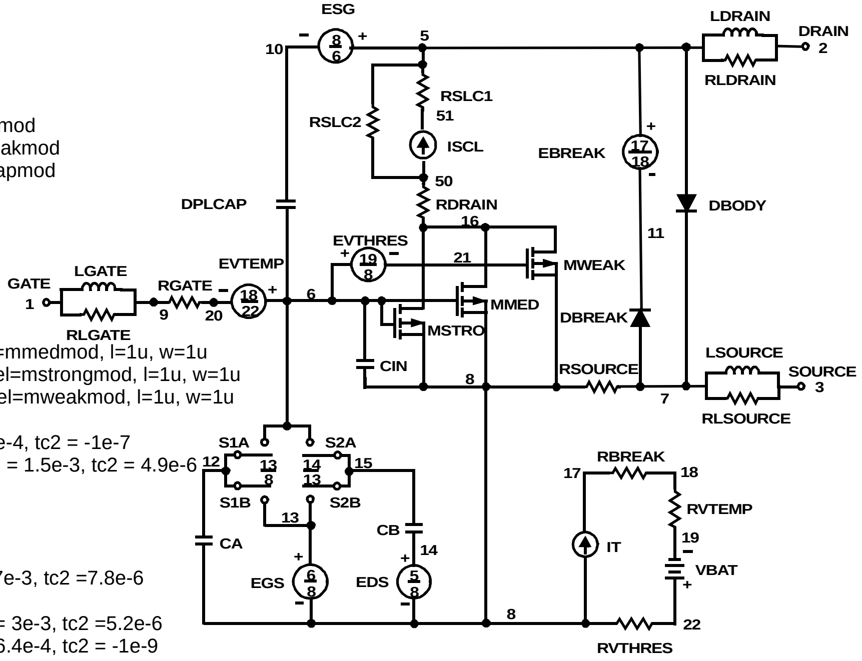


```
.SUBCKT FDM606P  2 1 3 ;       rev Oct. 2001
CA  12  8 18.3e-10
CB  15  14 18.3e-10
CIN  6  8 19.8e-10

DBODY 5 7 DBODYMOD
DBREAK 7 11  DBREAKMOD
DPLCAP 10 6 DPLCAPMOD

EBREAK 5 11 17  18 -23.4
EDS  14  8  5  8 1
EGS  13  8  6  8 1
ESG 5 10 8 6 1
EVTHRES 6 21 19 8  1
EVTEMP 6 20 18 22 1

IT  8  17  1

LDRAIN 2 5 1e-9
LGATE 1  9 1.1e-9
LSOURCE  3  7 0.78e-9

MMED 16 6 8 8 MMEDMOD
MSTRO 16 6 8 8 MSTROMOD
MWEAK 16 21 8 8 MWEAKMOD

RBREAK  17  18  RBREAKMOD  1
RDRAIN 50 16 RDRAINMOD 8.5e-3
RGATE  9  20 16
RLDRAIN 2 5 10
RLGATE 1 9 11
RLSOURCE 3 7 7.8
RSLC1 5 51 RSLCMOD 1e-6
RSLC2 5 50 1e3
RSOURCE  8  7  RSOURCEMOD 11e-3
RVTHRES 22 8 RVTHRESMOD  1
RVTEMP 18 19 RVTEMPMOD 1

S1A  6  12  13  8  S1AMOD
S1B  13  12  13  8  S1BMOD
S2A  6  15  14  13  S2AMOD
S2B  13  15  14  13  S2BMOD

VBAT 22 19  DC  1

ESLC 51 50 VALUE={(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51)/(1e-6*97),2.5))}

.MODEL DBODYMOD D (IS = 8e-11 N=1.07  RS = 1.3e-2  TRS1 = 1e-3  TRS2 = 1e-6  XTI=0  IKF=0.2  CJO = 5.9e-10  TT = 14.5e-9
 M = 0.47)
.MODEL DBREAKMOD D (RS = 5.3e-1  TRS1 = 5.5e-3  TRS2 = -9e-5)
.MODEL DPLCAPMOD D (CJO = 9.4e-10  IS = 1e-30  N = 10 M = 0.73)
.MODEL MMEDMOD PMOS (VTO = -0.96  KP = 1.3  IS=1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 16)
.MODEL MSTROMOD PMOS (VTO = -1.22  KP = 54  IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u)
.MODEL MWEAKMOD PMOS (VTO = -0.8  KP = 0.05 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 160 RS = 0.1)
.MODEL RBREAKMOD RES (TC1 = 7e-4  TC2 = -1e-7)
.MODEL RDRAINMOD RES (TC1 = 1.5e-3  TC2 = 4.9e-6)
.MODEL RSLCMOD RES (TC1 = 3.7e-3 TC2 = 7.8e-6)
.MODEL RSOURCEMOD RES (TC1 = 3e-3 TC2 = 5.2e-6)
.MODEL RVTHRESMOD RES (TC1 = 1.2e-3 TC2 = 1.2e-6)
.MODEL RVTEMPMOD RES (TC1 = -6.4e-4  TC2 = -1e-9)

.MODEL S1AMOD VSWITCH (RON = 1e-5  ROFF = 0.1  VON = 3.0  VOFF= 1.0)
.MODEL S1BMOD VSWITCH (RON = 1e-5  ROFF = 0.1  VON = 1.0  VOFF= 3.0)
.MODEL S2AMOD VSWITCH (RON = 1e-5  ROFF = 0.1  VON = 0.5  VOFF= -0.3)
.MODEL S2BMOD VSWITCH (RON = 1e-5  ROFF = 0.1  VON = -0.3  VOFF= 0.5)

.ENDS
```

Note: For further discussion of the PSPICE model, consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records, 1991, written by William J. Hepp and C. Frank Wheatley.

SABER Electrical Model

```
REV October 2001
template fdm606p n2,n1,n3
electrical n2,n1,n3
{
var i iscl
dp..model dbodymod = (isl = 8.0e-11, nl=1.07, rs = 1.3e-2, trs1 = 1e-3, trs2 = 1e-6, xti=0, cjo = 5.9e-10, ikf=0.2, tt = 14.5e-9, m = 0.47)
dp..model dbreakmod = (rs = 5.3e-1, trs1 = 5.5e-3, trs2 = -9.0e-5)
dp..model dplcapmod = (cjo = 9.4e-10, isl=10e-30, nl=10, m=0.73)
m..model mmedmod = (type=_p, vto = -0.96, kp=1.3, is=1e-30, tox=1)
m..model mstrongmod = (type=_p, vto = -1.22, kp = 54, is = 1e-30, tox = 1)
m..model mweakmod = (type=_p, vto = -0.8, kp = 0.05, is = 1e-30, tox = 1, rs=0.1)
sw_vcsp..model s1amod = (ron = 1e-5, roff = 0.1, von = 3.0, voff = 1.0)
sw_vcsp..model s1bmod = (ron = 1e-5, roff = 0.1, von = 1.0, voff = 3.0)
sw_vcsp..model s2amod = (ron = 1e-5, roff = 0.1, von = 0.5, voff = -0.3)
sw_vcsp..model s2bmod = (ron = 1e-5, roff = 0.1, von = -0.3, voff = 0.5)

c.ca n12 n8 = 18.3e-10
c.cb n15 n14 = 18.3e-10
c.cin n6 n8 = 19.8e-10

dp.dbody n5 n7 = model=dbodymod
dp.dbreak n7 n11 = model=dbreakmod
dp.dplcap n10 n6 = model=dplcapmod

i.it n8 n17 = 1

l.ldrain n2 n5 = 1e-9
l.lgate n1 n9 = 1.1e-9
l.lsource n3 n7 = 0.78e-9

m.mmed n16 n6 n8 n8 = model=mmedmod, l=1u, w=1u
m.mstrong n16 n6 n8 n8 = model=mstrongmod, l=1u, w=1u
m.mweak n16 n21 n8 n8 = model=mweakmod, l=1u, w=1u

res.rbreak n17 n18 = 1, tc1 = 7e-4, tc2 = -1e-7
res.rdrain n50 n16 = 8.5e-3, tc1 = 1.5e-3, tc2 = 4.9e-6
res.rgate n9 n20 = 16
res.rldrain n2 n5 = 10
res.rlgate n1 n9 = 11
res.rlsource n3 n7 = 7.8
res.rslc1 n5 n51= 1e-6, tc1 = 3.7e-3, tc2 =7.8e-6
res.rslc2 n5 n50 = 1e3
res.rsource n8 n7 = 11e-3, tc1 = 3e-3, tc2 =5.2e-6
res.rvtemp n18 n19 = 1, tc1 = -6.4e-4, tc2 = -1e-9
res.rvthres n22 n8 = 1, tc1 = 1.2e-3, tc2 = 1.2e-6

spe.ebreak n5 n11 n17 n18 = -23.4
spe.eds n14 n8 n5 n8 = 1
spe.egs n13 n8 n6 n8 = 1
spe.esg n5 n10 n6 n8 = 1
spe.evtemp n20 n6 n18 n22 = 1
spe.evthres n6 n21 n19 n8 = 1

sw_vcsp.s1a n6 n12 n13 n8 = model=s1amod
sw_vcsp.s1b n13 n12 n13 n8 = model=s1bmod
sw_vcsp.s2a n6 n15 n14 n13 = model=s2amod
sw_vcsp.s2b n13 n15 n14 n13 = model=s2bmod

v.vbat n22 n19 = dc=1

equations {
i (n51->n50) +=iscl
iscl: v(n51,n50) = ((v(n5,n51)/(1e-9+abs(v(n5,n51))))*((abs(v(n5,n51)*1e6/97))** 2.5))
}
}
```

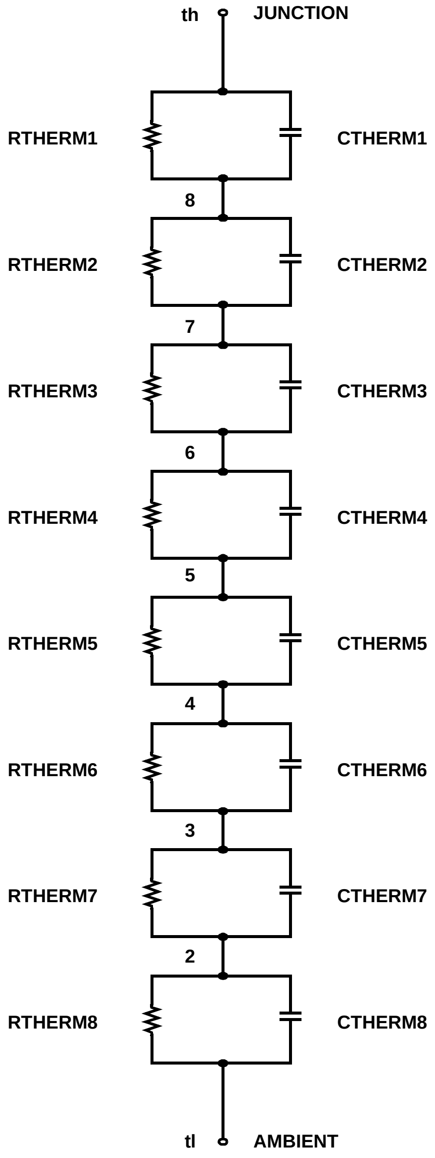


SPICE Thermal Model

```
REV October 2001
FDM606P_JA Junction Ambient
Copper Area= 1sq.in

CTHERM1 Junction c2 2e-4
CTHERM2 c2 c3 3.0e-4
CTHERM3 c3 c4 7.0e-4
CTHERM4 c4 c5 2.0e-3
CTHERM5 c5 c6 6.4e-3
CTHERM6 c6 c7 3.0e-2
CTHERM7 c7 c8 2.8e-1
CTHERM8 c8 Ambient 2.9

RTHERM1 Junction c2 1.0
RTHERM2 c2 c3 1.3
RTHERM3 c3 c4 2.5
RTHERM4 c4 c5 3.0
RTHERM5 c5 c6 4.0
RTHERM6 c6 c7 7.7
RTHERM7 c7 c8 12.7
RTHERM8 c8 Ambient 24
```

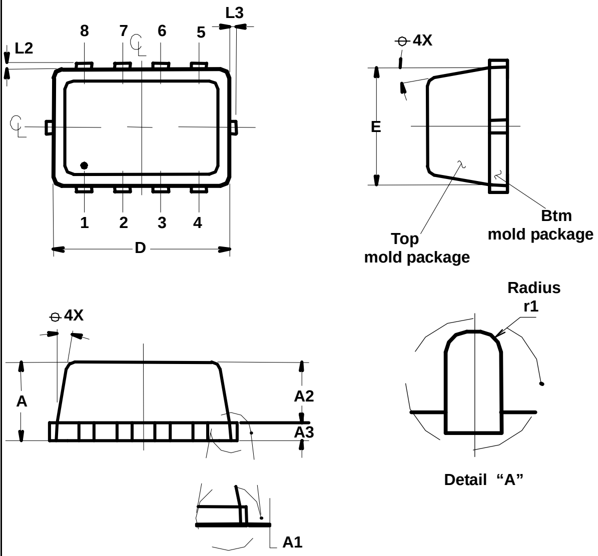
SABER Thermal Model

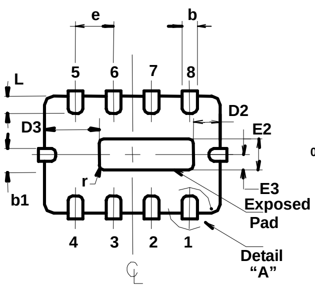
```
SABER thermal model FDM606P
Copper Area= 1sq.in
template thermal_model th tl
thermal_c th, tl
{
ctherm.ctherm1 th c2 = 2.0e-4
ctherm.ctherm2 c2 c3 = 3.0e-4
ctherm.ctherm3 c3 c4 = 7.0e-4
ctherm.ctherm4 c4 c5 = 2.0e-3
ctherm.ctherm5 c5 c6 = 6.4e-3
ctherm.ctherm6 c6 c7 = 3.0e-2
ctherm.ctherm7 c7 c8 = 2.8e-1
ctherm.ctherm8 c8 tl = 2.9

rtherm.rtherm1 th c2 = 1.0
rtherm.rtherm2 c2 c3 = 1.3
rtherm.rtherm3 c3 c4 = 2.5
rtherm.rtherm4 c4 c5 = 3.0
rtherm.rtherm5 c5 c6 = 4.0
rtherm.rtherm6 c6 c7 = 7.7
rtherm.rtherm7 c7 c8 = 12.7
rtherm.rtherm8 c8 tl = 24
}
```

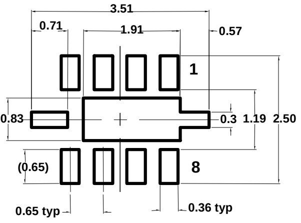


MicroFET 3x2-8

SURFACE MOUNT JEDEC MicroFET 3x2-8 PLASTIC PACKAGE







Recommended land pattern

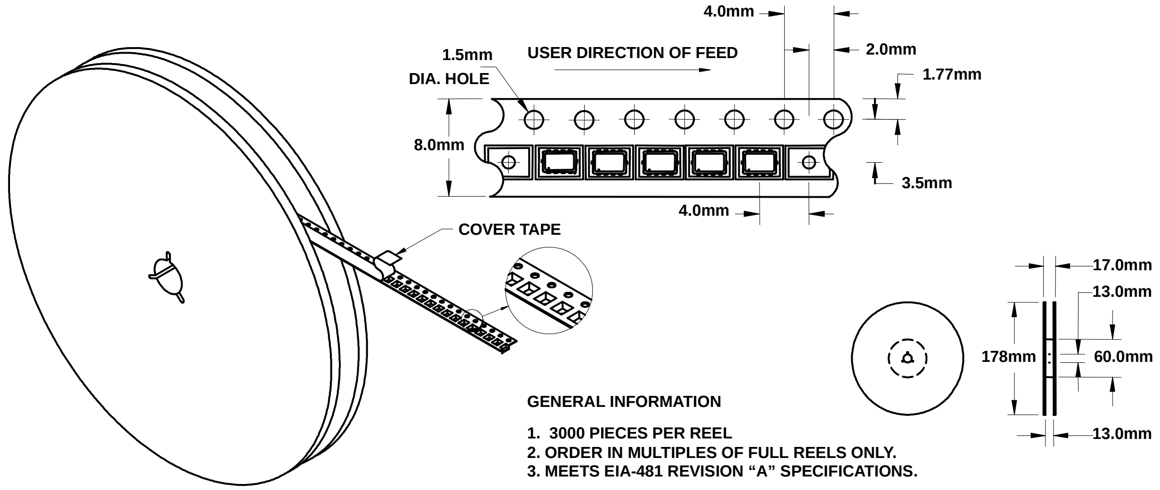
SYMBOL	MILLIMETERS		NOTES
	MIN	MAX	
A	0.80	1.00	1
A1	0.00	0.05	1
A2	0.65	0.75	1
A3	0.15	0.25	1
b	0.12	0.28	1
b1	0.24	0.50	1
D	2.90	3.10	1
E	1.90	2.10	1
D2	0.46	0.61	1
E2	0.45	0.60	1
D3	0.91	1.02	1
E3	0.15	0.35	1
e	0.65 BSC		1
L	0.21	0.37	1
L2	0.00	0.10	1
L3	0.00	0.10	1
N	8		4
r	0.127 BSC		1
r1	0.127 BSC		1
Ø	0^o	12^o	

NOTES:

1. All dimensions are in mm.
2. Package outline exclusive of mold flash & metal burr.
3. Package outine inclusive of plating.
4. N is the total number of terminals.
5. Package surface finishing of Ra 0.4 um max.

MicroFET 3x2-8

8mm TAPE REEL



GENERAL INFORMATION

1. 3000 PIECES PER REEL
2. ORDER IN MULTIPLES OF FULL REELS ONLY.
3. MEETS EIA-481 REVISION "A" SPECIFICATIONS.

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