MAX11192

12-Bit, 2Msps, Dual Simultaneous Sampling SAR ADCs with Internal Reference

General Description

The MAX11192 is a dual-channel SAR ADC with simultaneous sampling at 2Msps, 12-bit resolution, and differential inputs. Available in a tiny 16-pin, 3mm x 2mm ultra TDFN package, this ADC delivers excellent static and dynamic performance while operating from a supply voltage over the range of 3.0V to 5.25V. An integrated reference further reduces board area and component count.

The MAX11192 achieves 73dB of SNR (min), -108dB of THD (typ), and INL less than ±0.5LSB with no missing codes. The SPI-compatible serial interface includes a separate data output for each channel. Specifications apply over the extended industrial temperature range of -40°C to +125°C.

Applications

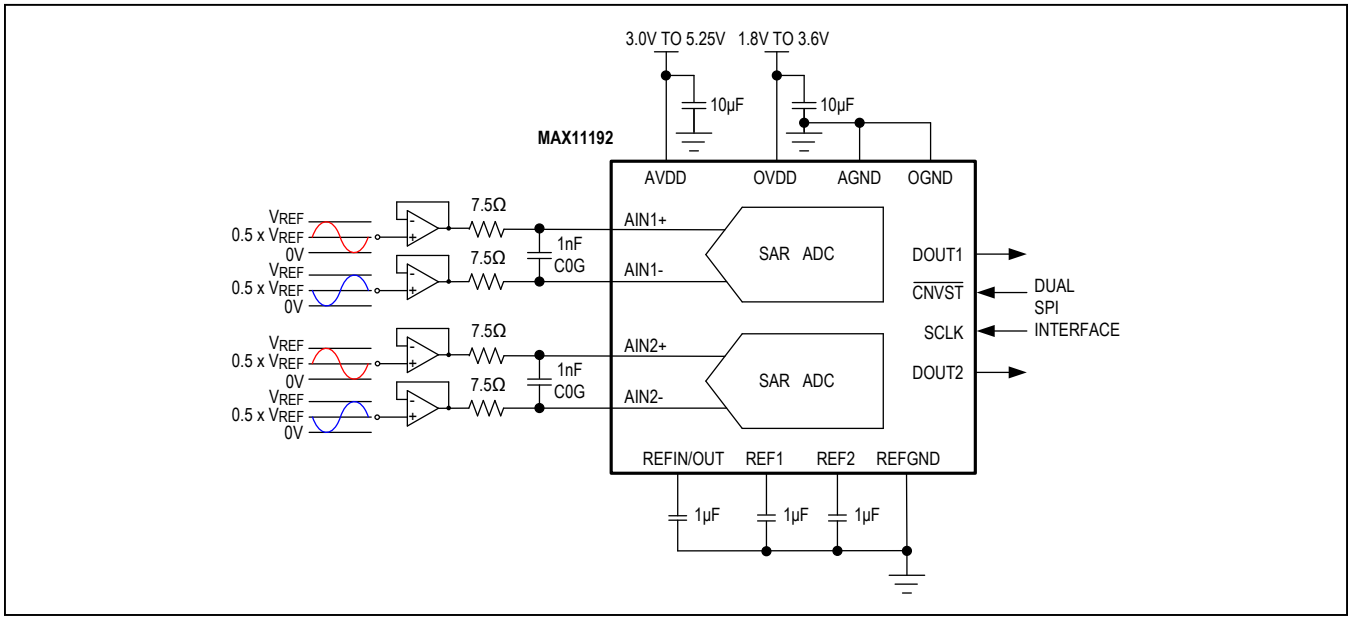
- Encoders
- Resolvers
- LVDT
- Current Sensing in Motors
- PLC

Benefits and Features

- Tiny 16-Pin, 3mm x 2mm, Ultra TDFN Package
- Up to 2Msps Throughput Rate
- Two Simultaneous-Sampling ADC Cores
- 2.5V Integrated Reference and Reference Buffers
- Two Data Outputs for the Two Simultaneous-Sampling ADCs
- No Overhead Clock Cycles; 12 Clock Cycles for 12-Bit Result
- Balanced, Differential Input Range of ±V_{REF}
- 73dB SNR (min), -108dB THD (typ) at 10kHz
- INL < ±0.5LSB, No Missing Codes

Ordering Information appears at end of data sheet.

Application Diagram



Absolute Maximum Ratings

AVDD to GND, REFGND, OGND .....-0.3V to +5.5V
OVDD to GND, REFGND, OGND.....-0.3V to +5.5V
AINn+, AINn- to GND, REFGND, OGND.. -0.3V to The lower of (V_{AVDD} + 0.3V) and +5.5V
REFIN, REF1, REF2 to GND, REFGND, OGND.....-0.3V to The lower of (V_{AVDD} + 0.3V) and +5.5V
$\overline{CNVST}$, SCLK, DOUT1, DOUT2 to OGND.....-0.3V to The lower of (V_{OVDD} + 0.3V) and +5.5V
GND to REFGND to OGND .....-0.3V to +0.3V
Maximum Current Into Any Pin ..... -50mA to +50mA
Continuous Power Dissipation (16 UTDFN; T_A = +70°C; derate 16.7mW/°C above +70°C) ( ).....1333mW
Operating Temperature Range.....-40°C to 125°C
Junction Temperature.....+150°C
Storage Temperature Range..... -65°C to +150°C
Lead Temperature (soldering, 10s) .....+300ºC
Soldering Temperature (reflow).....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

16 Ultra TDFN

PACKAGE CODE	T1623CN+1
Outline Number	21-100030
Land Pattern Number	—
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	60
Junction to Case (θ_{JC})	11

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

Electrical Characteristics

(f_{Sample} = 2MSPS; V_{AVDD} = 5.0V, V_{OVDD} = 1.8V; $V_{REFIN/OUT}$ = 2.5V (Internal Reference); T_A = T_{MIN} to T_{MAX} (Note 1). Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ANALOG INPUTS						
Input Voltage Range	$V_{IN(DIFF)}$	AINn+ – AINn-		±V_{REF}		V
Absolute Input Voltage Range	$V_{IN(RNG)}$	AINn+/AINn- relative to GND	-0.1		V_{AVDD} + 0.1	V
Common-Mode Input Voltage Range	CMI_{RNG}	(AINn+ + AINn-)/2	V_{REF}/2 - 0.1		V_{REF}/2 + 0.1	V
Input Leakage Current	I_{IN_LEAK}	Acquisition phase		1		µA
Input Capacitance	C_{IN}			10		pF

Electrical Characteristics (continued)

(f_{Sample} = 2MSPS; V_{AVDD} = 5.0V, V_{OVDD} = 1.8V; $V_{REFIN/OUT}$ = 2.5V (Internal Reference); T_A = T_{MIN} to T_{MAX} (Note 1). Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STATIC PERFORMANCE (VREFIN/OUT = 2.5V, INTERNAL REFERENCE)						
Resolution	N		12			Bits
No Missing Codes			12			Bits
Offset Error	OE		-1		+1	LSB
Offset Error TC				1.2		mLSB/°C
Gain Error	GE	(Note 2)	-1		+1	LSB
Gain Error TC		(Note 2)		1.2		mLSB/°C
Integral Nonlinearity	INL		-0.5		+0.5	LSB
Differential Nonlinearity	DNL		-0.25		+0.25	LSB
Analog Input CMR		Common Mode Range; $V_{REF}/2$ - 100mV to $V_{REF}/2$ + 100mV		40		mLSB/V
Power-Supply Rejection	PSRR	AVDD		3		LSB/V
Power Supply Rejection	PSRR	OVDD		3		LSB/V
INTERNAL REFERENCE						
Initial Accuracy		T_A = +25°C	2.498	2.500	2.502	V
Temperature Drift				5		ppm
EXTERNAL REFERENCE						
Input Voltage Range		External reference applied to REFIN	2.5		V_{AVDD} - 0.25	
		External reference applied to REF1 or REF2	2.5		V_{AVDD} + 0.1	V
REFERENCE BUFFERS						
Bypass Capacitor			4.7			µF
DYNAMIC PERFORMANCE (VREFIN/OUT = 2.5V, INTERNAL REFERENCE)						
Signal-to-Noise Ratio	SNR	10kHz input	73			dB
Signal-to-Noise And Distortion Ratio	SINAD	10kHz input		73.5		dB
Spurious-Free Dynamic Range	SFDR	10kHz input		102		dB
Total Harmonic Distortion	THD	10kHz input		-108		dB
Crossalk		10kHz input		-100		dB
DYNAMIC PERFORMANCE (VREFIN/OUT = 4.096V, EXTERNAL REFERENCE)						
Signal-to-Noise Ratio	SNR	10kHz input	73			dB
Signal-to-Noise And Distortion Ratio	SINAD	10kHz input		73.5		dB
Spurious-Free Dynamic Range	SFDR	10kHz input		102		dB
Total Harmonic Distortion	THD	10kHz input		-108		dB
Crossalk		10kHz input		-100		dB
SAMPLING DYNAMICS						
Throughput					2	Msps
Aperture Delay Match				150		ps
Input -3db Bandwidth	f_{-3dB}			50		MHz

Electrical Characteristics (continued)

(f_{Sample} = 2MSPS; V_{AVDD} = 5.0V, V_{OVDD} = 1.8V; $V_{REFIN/OUT}$ = 2.5V (Internal Reference); T_A = T_{MIN} to T_{MAX} (Note 1). Typical values are at T_A = +25°C, unless otherwise noted.)

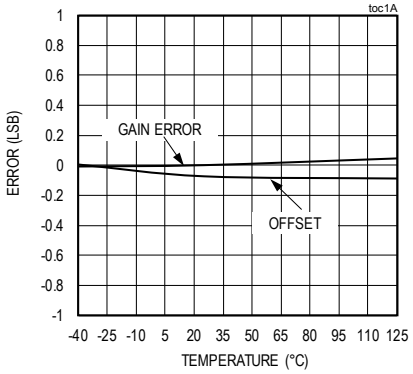
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLIES						
Analog Supply Voltage	AVDD		3.0	5.0	5.25	V
Interface Supply Voltage	OVDD		1.7		3.6	V
Analog Supply Current	I(AVDD)			5.5	7	mA
Interface Supply Current	I(OVDD)	DOUT load: C_{LOAD} = 10pF		0.75	1	mA
Analog Standby Current	I_S(AVDD)	(Note 3)		1		mA
Interface Standby Current	I_S(OVDD)	(Note 3)		1		µA
DIGITAL INPUTS						
Input Voltage High	V_{IH}		0.8 x V_{OVDD}			V
Input Voltage Low	V_{IL}				0.2 x V_{OVDD}	V
Input Capacitance				2		pF
Input Leakage				1		µA
DIGITAL OUTPUTS						
Output Voltage High	V_{OH}	I_{SOURCE} = 2mA	V_{OVDD} - 0.4			V
Output Voltage Low	V_{OL}	I_{SINK} = 2mA			V_{OGND} + 0.4	V
TIMING						
Conversion Period	t_1		500			ns
SCLK to DOUT Hold	t_2		1			ns
SCLK to DOUT Valid	t_3		14			ns
SCLK High	t_4		8			ns
SCLK Period	t_5		20			ns
SCLK low	t_6		8			ns
$\overline{CNVST}$ Rising Edge to SCLK Rising Edge	t_7		5			ns
SCLK Rising Edge to $\overline{CNVST}$ Rising Edge	t_8		5			ns
$\overline{CNVST}$ High	t_9		60			ns
$\overline{CNVST}$ Falling Edge to SCLK Rising Edge	t_{10}		10			ns
SCLK Falling Edge to $\overline{CNVST}$ Falling Edge	t_{11}		0			ns
$\overline{CNVST}$ Low Time for Valid Sample	t_{12}		400			ns

Note 1: Units are 100% production tested at TA = +25°C and are guaranteed by design and characterization from T_A = T_{MIN} to T_{MAX}.
Note 2: Exclude the reference drift and offset error.
Note 3: This current is drawn when the device has completed conversion and SCLK is idle.

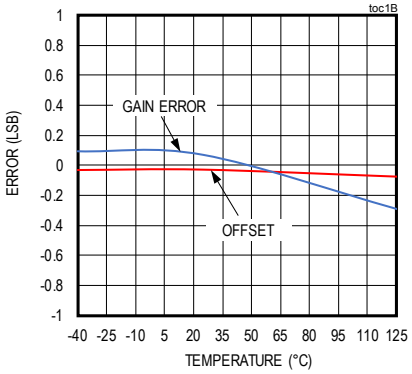
Typical Operating Characteristics

(f_{SAMPLE} = 2Msps; V_{AVDD} = 5.0V, V_{OVDD} = 1.8V; $V_{REFIN/OUT}$ = 2.5V (Internal Reference); T_A = T_{MIN} to T_{MAX}. Typical values are at T_A = +25ºC, unless otherwise noted.)

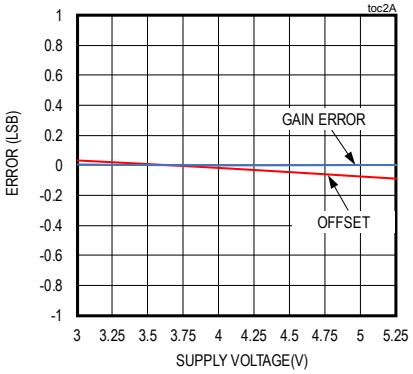
OFFSET AND GAIN ERROR vs. TEMPERATURE (CHANNEL A)



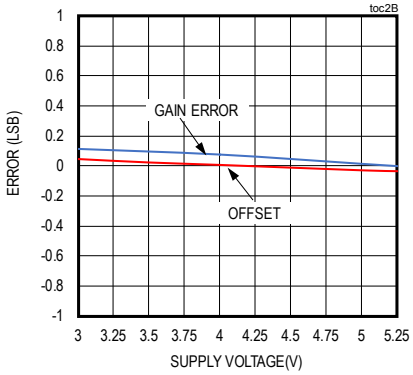
OFFSET AND GAIN ERROR vs. TEMPERATURE (CHANNEL B)



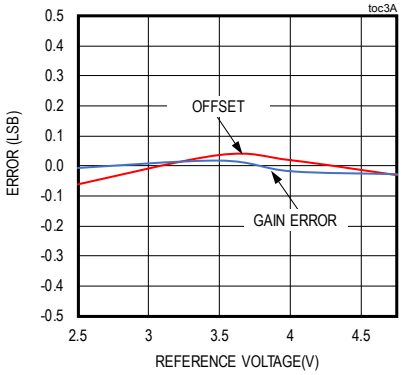
OFFSET AND GAIN ERROR vs. SUPPLY VOLTAGE (CHANNEL A)



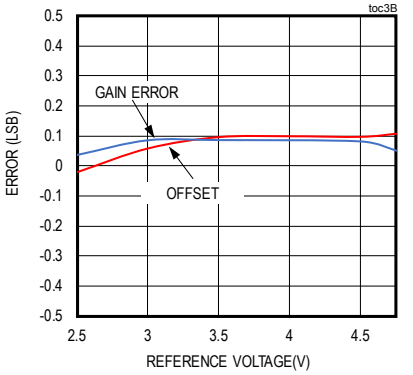
OFFSET AND GAIN ERROR vs. SUPPLY VOLTAGE (CHANNEL B)



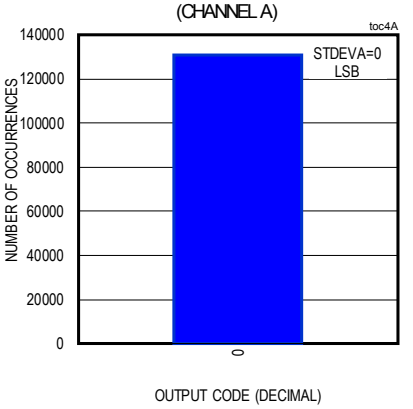
OFFSET AND GAIN ERROR vs. REFERENCE VOLTAGE (CHANNEL A)



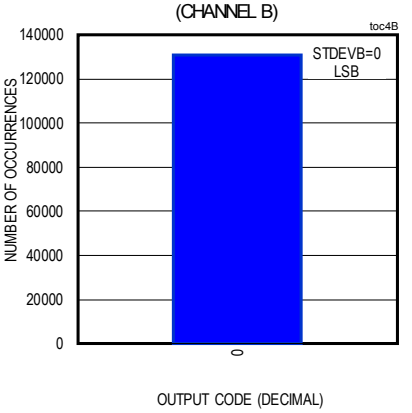
OFFSET AND GAIN ERROR vs. REFERENCE VOLTAGE (CHANNEL B)



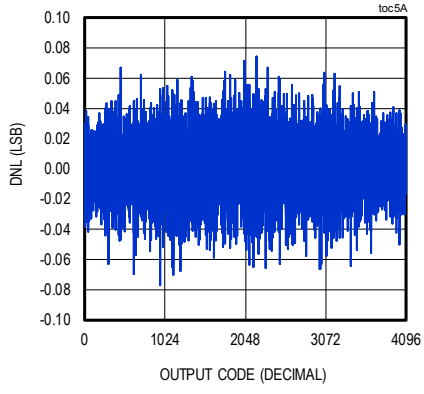
OUTPUT NOISE HISTOGRAM (CHANNEL A)



OUTPUT NOISE HISTOGRAM (CHANNEL B)



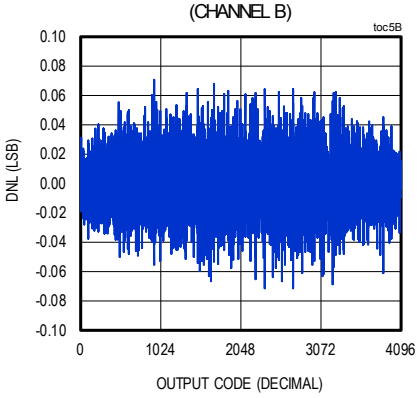
DNL vs. CODE (CHANNEL A)



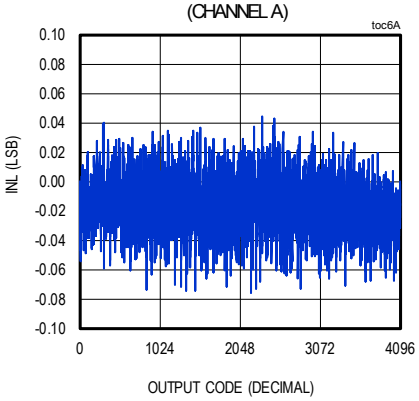
Typical Operating Characteristics (continued)

(f_{SAMPLE} = 2Msps; V_{AVDD} = 5.0V, V_{OVDD} = 1.8V; $V_{REFIN/OUT}$ = 2.5V (Internal Reference); T_A = T_{MIN} to T_{MAX}. Typical values are at T_A = +25ºC, unless otherwise noted.)

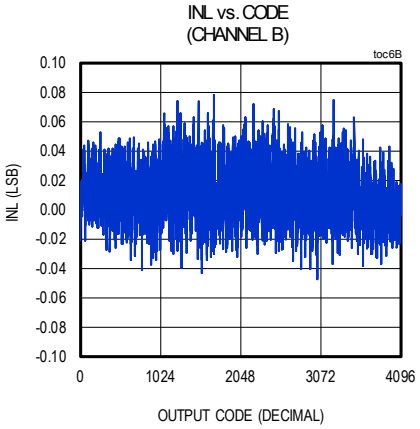
DNL vs. CODE (CHANNEL B)



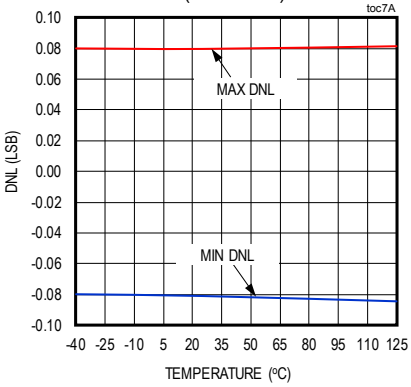
INL vs. CODE (CHANNEL A)



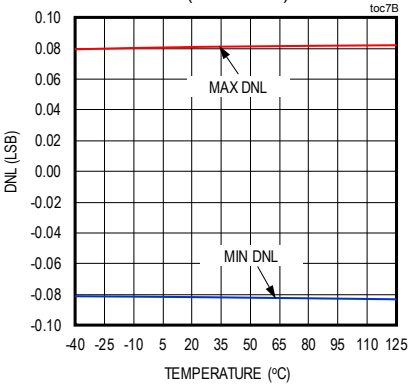
INL vs. CODE (CHANNEL B)



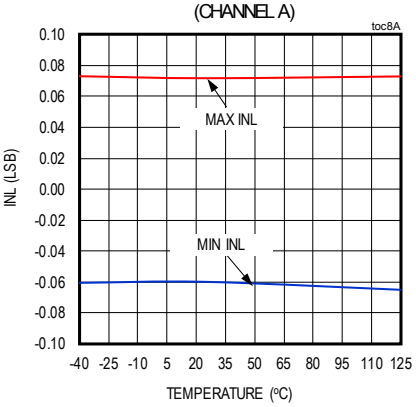
DNL vs. TEMPERATURE (CHANNEL A)



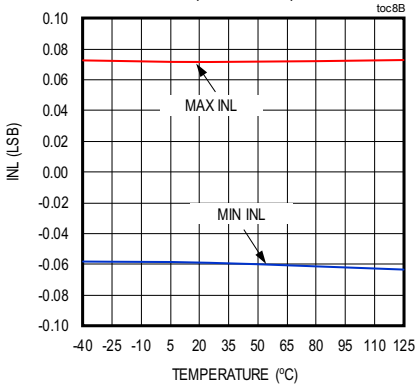
DNL vs. TEMPERATURE (CHANNEL B)



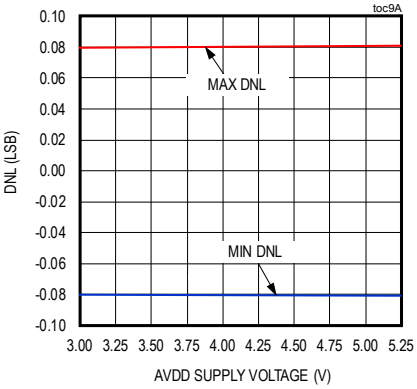
INL vs. TEMPERATURE (CHANNEL A)



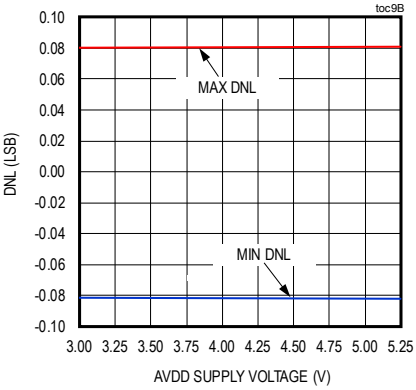
INL vs. TEMPERATURE (CHANNEL B)



DNL vs. AVDD SUPPLY VOLTAGE (CHANNEL A)



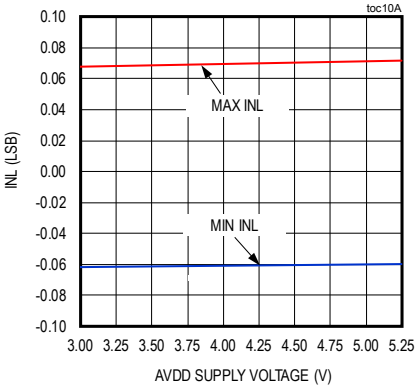
DNL vs. AVDD SUPPLY VOLTAGE (CHANNEL B)



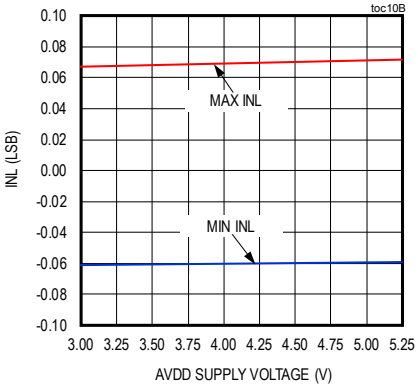
Typical Operating Characteristics (continued)

(f_{SAMPLE} = 2Msps; V_{AVDD} = 5.0V, V_{OVDD} = 1.8V; $V_{REFIN/OUT}$ = 2.5V (Internal Reference); T_A = T_{MIN} to T_{MAX}. Typical values are at T_A = +25ºC, unless otherwise noted.)

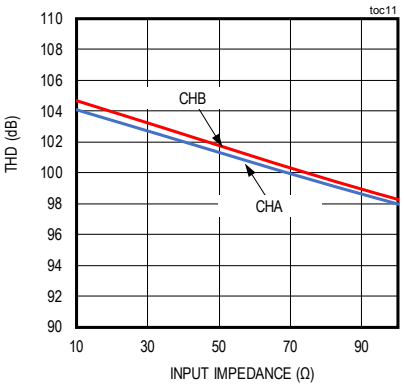
INL vs. AVDD SUPPLY VOLTAGE (CHANNEL A)



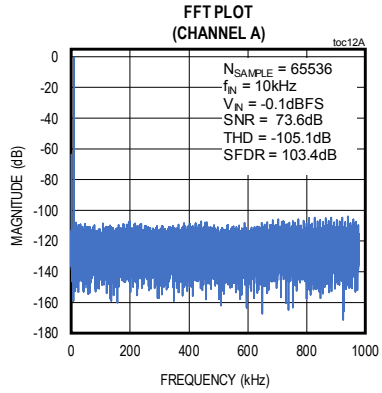
INL vs. AVDD SUPPLY VOLTAGE (CHANNEL B)



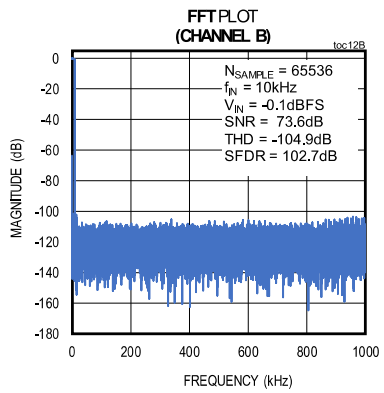
THD vs. INPUT IMPEDANCE



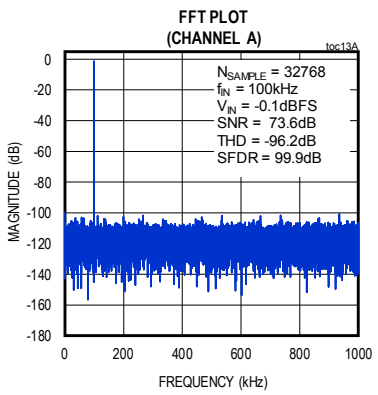
FFT PLOT (CHANNEL A)



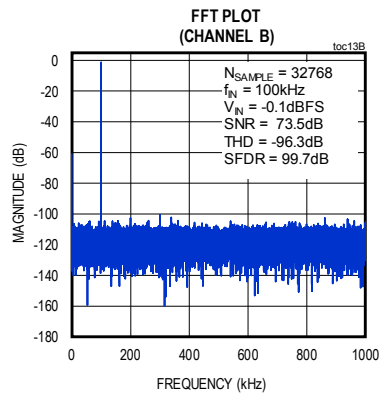
FFT PLOT (CHANNEL B)



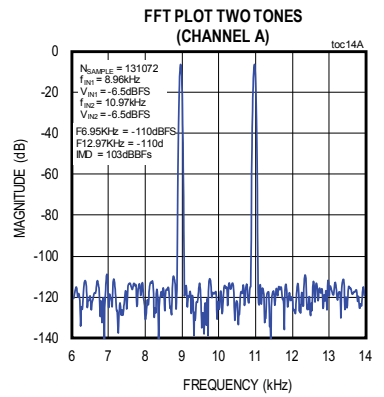
FFT PLOT (CHANNEL A)



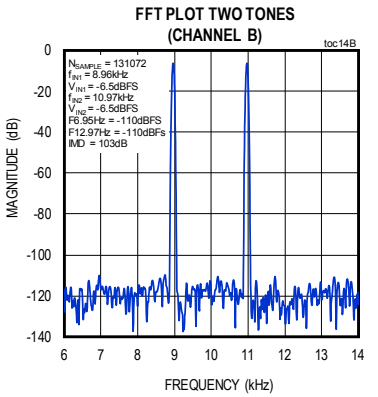
FFT PLOT (CHANNEL B)



FFT PLOT TWO TONES (CHANNEL A)



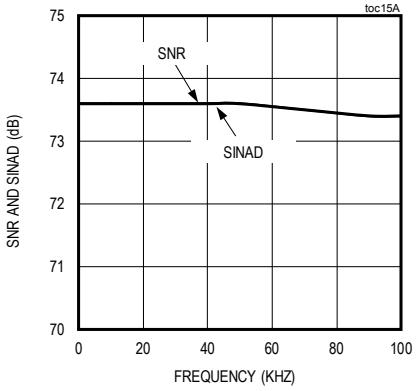
FFT PLOT TWO TONES (CHANNEL B)



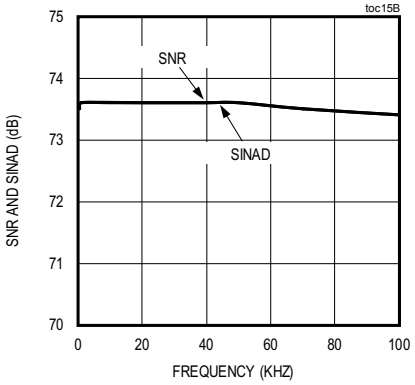
Typical Operating Characteristics (continued)

(f_{SAMPLE} = 2Msps; V_{AVDD} = 5.0V, V_{OVDD} = 1.8V; $V_{REFIN/OUT}$ = 2.5V (Internal Reference); T_A = T_{MIN} to T_{MAX}. Typical values are at T_A = +25ºC, unless otherwise noted.)

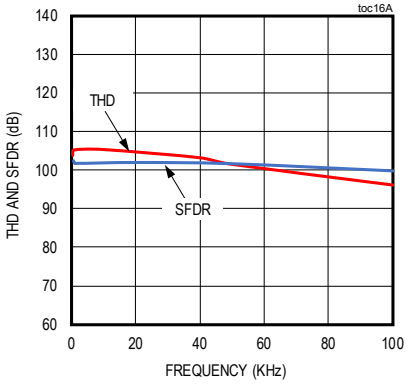
SNR AND SINAD vs. FREQUENCY (CHANNEL A)



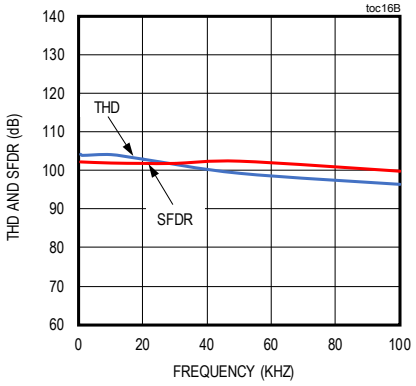
SNR AND SINAD vs. FREQUENCY (CHANNEL B)



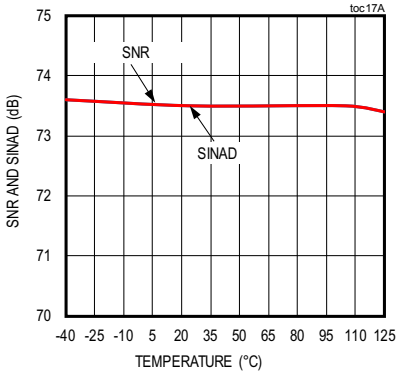
THD AND SFDR vs. FREQUENCY (CHANNEL A)



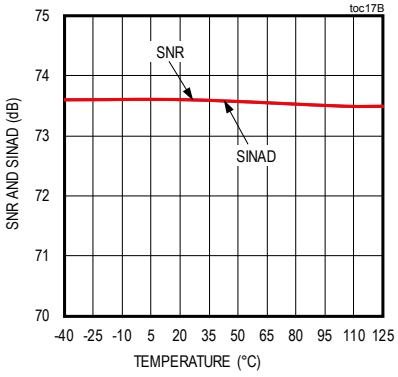
THD AND SFDR vs. FREQUENCY (CHANNEL B)



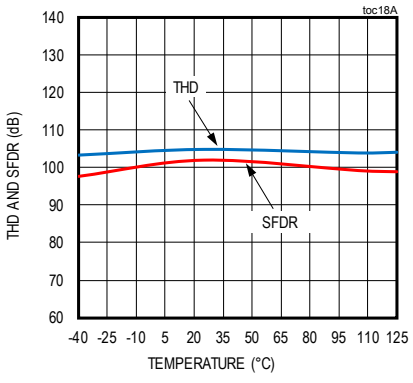
SNR AND SINAD vs. TEMPERATURE (CHANNEL A)



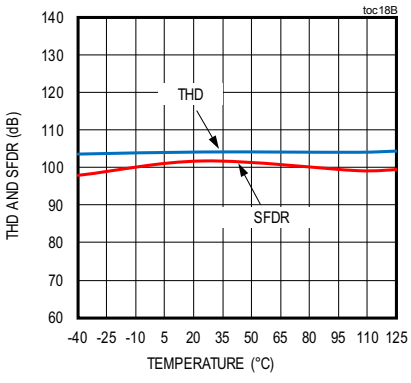
SNR AND SINAD vs. TEMPERATURE (CHANNEL B)



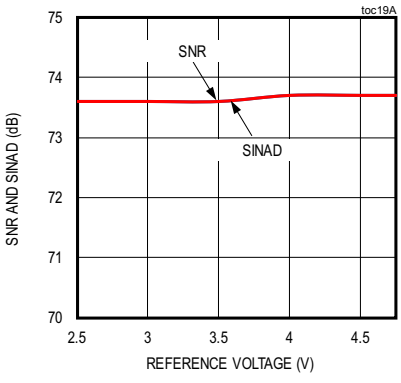
THD AND SFDR vs. TEMPERATURE (CHANNEL A)



THD AND SFDR vs. TEMPERATURE (CHANNEL B)



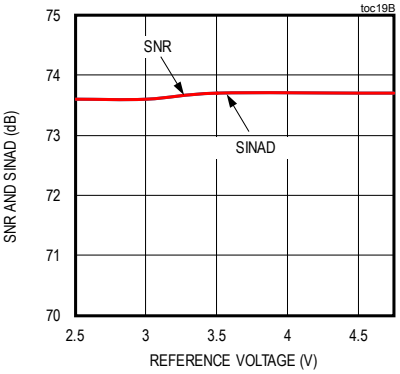
SNR AND SINAD vs. REFERENCE VOLTAGE (CHANNEL A)



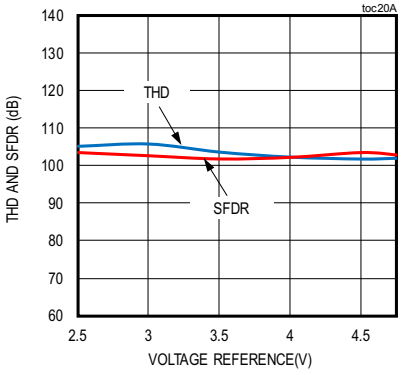
Typical Operating Characteristics (continued)

(f_{SAMPLE} = 2Msps; V_{AVDD} = 5.0V, V_{OVDD} = 1.8V; $V_{REFIN/OUT}$ = 2.5V (Internal Reference); T_A = T_{MIN} to T_{MAX}. Typical values are at T_A = +25ºC, unless otherwise noted.)

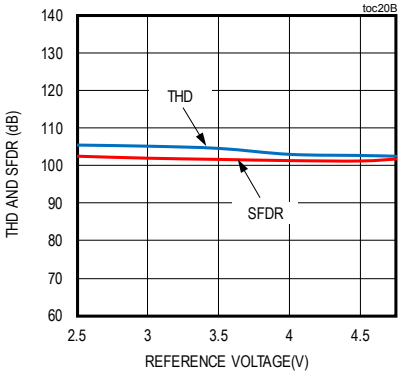
SNR AND SINAD vs. REFERENCE VOLTAGE (CHANNEL B)



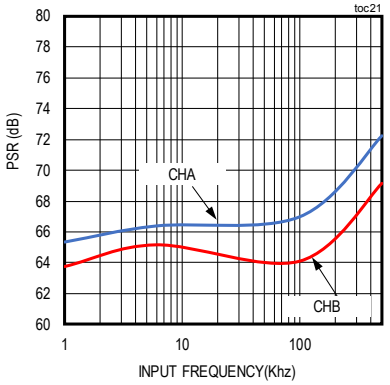
THD AND SFDR vs. REFERENCE VOLTAGE (CHANNEL A)



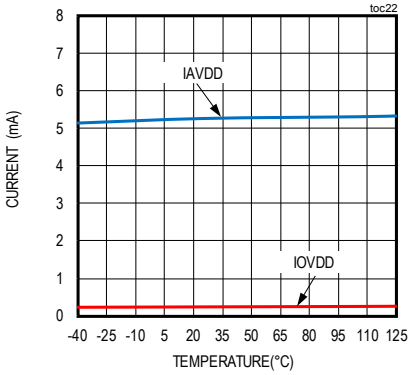
THD AND SFDR vs. REFERENCE VOLTAGE (CHANNEL B)



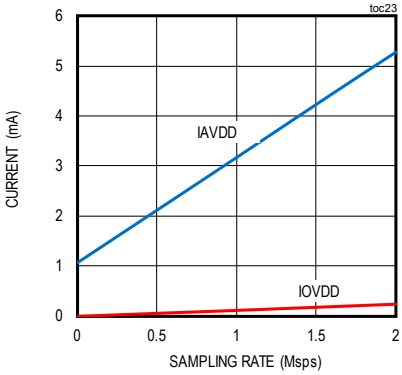
PSR vs. INPUT FREQUENCY



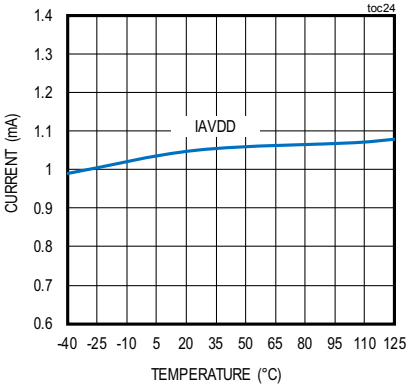
CURRENT vs. TEMPERATURE



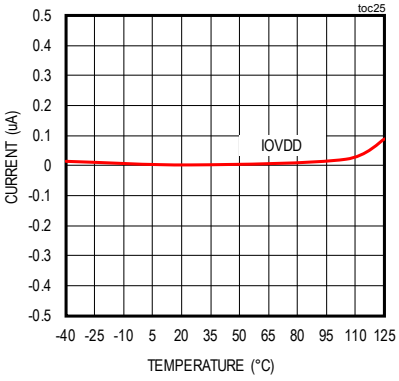
CURRENT vs. SAMPLING RATE



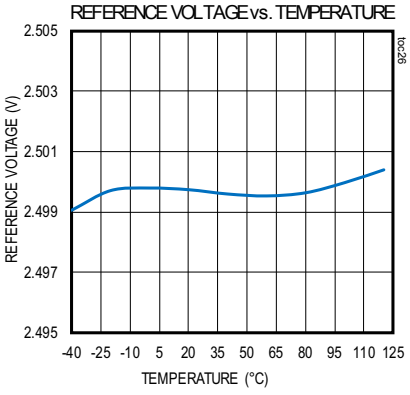
AVDD STANDBY CURRENT vs. TEMPERATURE



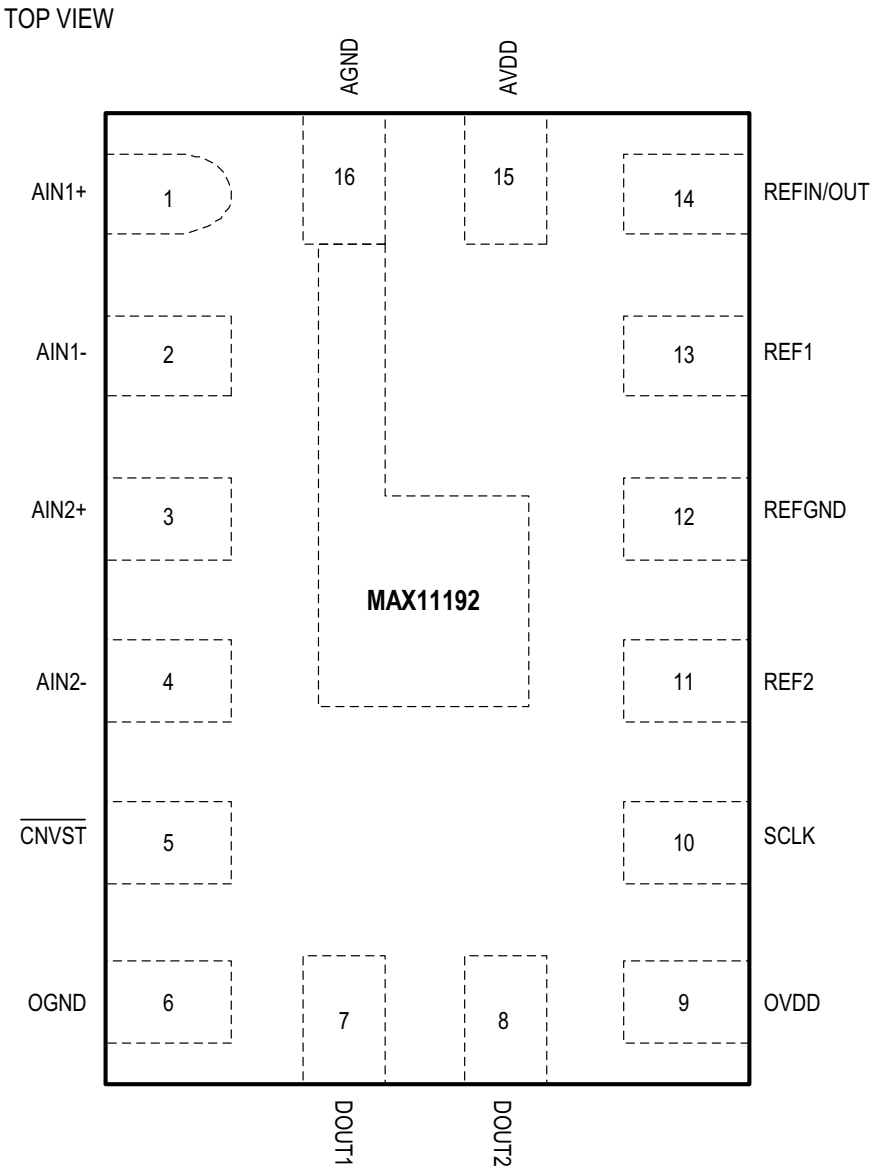
OVDD STANDBY CURRENT vs. TEMPERATURE



REFERENCE VOLTAGE vs. TEMPERATURE



Pin Configuration



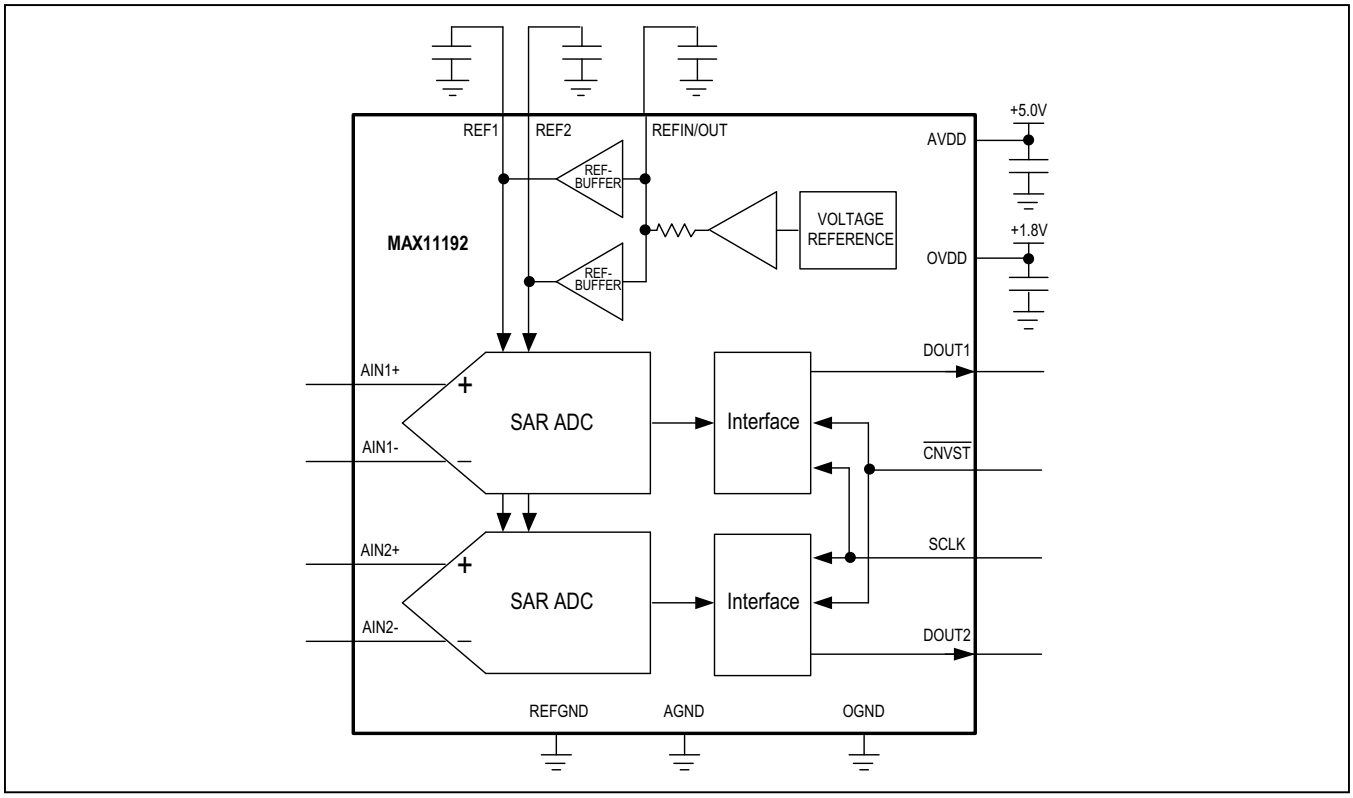
UTDFN
2mm x 3mm

EXPOSED PAD IS CONNECTED TO AGND

Pin Description

PIN	NAME	FUNCTION
1	AIN1+	ADC1 Positive (+) Analog Input
2	AIN1-	ADC1 Negative (-) Analog Input
3	AIN2+	ADC2 Positive (+) Analog Input
4	AIN2-	ADC2 Negative (-) Analog Input
5	$\overline{\text{CNVST}}$	Conversion Start Input
6	OGND	Ground (IO Ground)
7	DOUT1	Serial Interface Data Out for ADC1
8	DOUT2	Serial Interface Data Out for ADC2
9	OVDD	IO Supply. Bypass with a 10µF capacitor to ground
10	SCLK	Serial Interface Clock
11	REF2	REF2 Bypass Pin. Bypass with a 1µF capacitor to ground
12	REFGND	Ground (Reference Ground)
13	REF1	REF1 Bypass Pin. Bypass with a 1µF capacitor to ground
14	REFIN/OUT	External Reference Input or Internal Reference Decoupling. Bypass with 1µF capacitor to ground
15	AVDD	Analog Supply Pin. Bypass with a 10µF capacitor to ground
16	AGND	Ground

Functional Diagram



Detailed Description

The MAX11192 is a 12-bit, 2-channel, 2Msps, SAR ADC with simultaneous sampling, balanced differential inputs, and a separate data output for each channel. This ADC features best-in-class sample rate and resolution in a tiny 2mm x 3mm package. An integrated voltage reference and reference buffers help to minimize board space, component count, and system cost. An internal oscillator sets conversion time, thereby simplifying external timing requirements.

For fast throughput, the SPI-compatible digital interface includes two data out pins (DOUT1 and DOUT2). DOUT1 provides conversion data from ADC1, while DOUT2 provides conversion data from ADC2. Data bits are clocked out on the rising edge of SCLK.

Analog Inputs

The analog inputs of the MAX11192, AINn+ and AINn-, should be driven with balanced differential signals. The input signals can range from 0V to V_{REF}. Thus, the differential input interval V_{DIFF} = (AINn+) - (AINn-) ranges from – V_{REF} to + V_{REF}, and the full-scale range is:

$$FSR = 2 \times V_{REF}$$

The nominal resolution step width of the least significant bit (LSB) is:

$$LSB = \frac{FSR}{2^N} = \frac{2 \times V_{REF}}{2^N}, \quad N = 12$$

The differential analog input must be centered with respect to a common mode signal of $V_{REF}/2$, with a tolerance of ±100mV. The reference voltage can range from 2.5V to 250mV below the reference supply AVDD. This will guarantee adequate headroom for the internal reference buffers. Figure 1 illustrates signal ranges for AINn+/AINn-, reference voltage V_{REF} and reference supply voltage AVDD.

Figure 2 shows the analog input equivalent circuit of MAX11192. The ADC samples both inputs, AINn+ and AINn-, with a differential on-chip track-and-hold exhibiting no pipeline delay or latency.

Each analog input (see Figure 2) has dedicated input clamps to protect from overranging. Diodes D1 and D2 provide ESD protection and act as a clamp for the input voltages. Diodes D1/D2 can sustain a maximum forward current of 100mA. The sampling switches connect the inputs to the sampling capacitors.

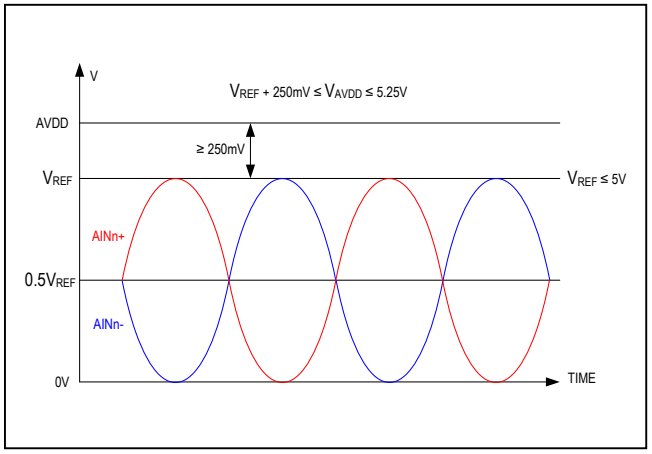


Figure 1. Input Signal Ranges

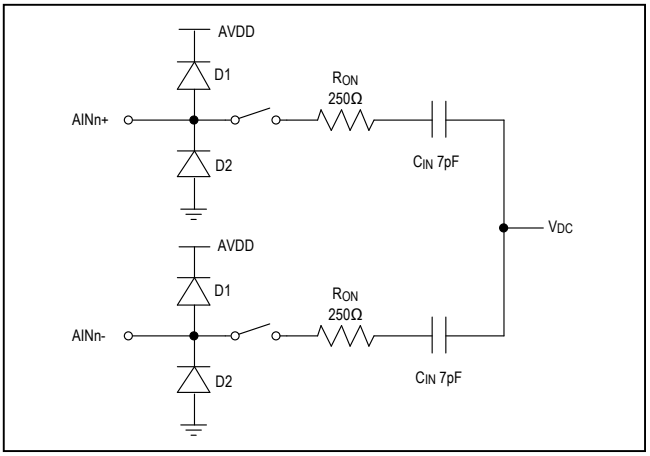


Figure 2. Simplified Model of Input Sampling Circuit

Input Settling

Figure 3 shows the timing of the conversion cycle's track, SAR conversion, and read data operations. In the track phase, starting with the rising edge of $\overline{CNVST}$, the sample switches are closed and the analog inputs are directly connected to the sample capacitors. The source resistance determines the charging of the sample capacitor to the input voltage. The falling edge of $\overline{CNVST}$ is the sampling instant for the ADCs. At this instant, the track phase ends, the sample switches open, and the ADC enters into the successive approximation (SAR) conversion phase. In the conversion phase, a comparator compares the voltage on the sample capacitor against the internal DAC value, which cycles through values of binary-weighted fractions of V_{REF} using the successive approximation technique. The final result is read through the SPI bus. Note that ADC1 and ADC2 operate in parallel and conversion data is available simultaneously through DOUT1 and DOUT2.

The ADCs go back into track phase on the rising edge of $\overline{CNVST}$. To achieve accurate conversion results, each ADC should track its input signal for an interval longer than the input signal's settling time. If the signal cannot settle within the allocated track time due to excessive source resistance, external ADC drivers are recommended to achieve faster settling. Note that, since the MAX11192 has a fixed conversion time set by an internal oscillator, reducing the sample rate can increase the track time.

The settling behavior is determined by the time constant in the sampling network. The time constant depends upon the total resistance (source resistance + switch resistance, R_{ON}) and total capacitance (sampling capacitor C_{IN}, external input capacitor, PCB parasitic capacitors, etc). Modeling the input circuit with a single pole network, the time constant, $R_{TOTAL} \times C_{LOAD}$, of the input should not exceed $t_{TRACK}/12$, where R_{TOTAL} is the total resistance (source resistance + switch resistance), C_{LOAD} is the total capacitance (sampling capacitor, external input capacitor, PCB parasitic capacitor), and t_{TRACK} is the track time.

When an ADC driver amplifier is used, it is recommended to use a series resistance (typically 5Ω to 50Ω) between the amplifier and the ADC inputs, as shown in the Application Diagram. The following are some of the requirements for the ADC driver amplifier.

1) Fast settling time: For a multichannel multiplexed circuit,the ADC driver amplifier must be able to settle with an error less than 0.5 LSB during the minimum track time when a full-scale step is applied.
2) Low noise: It is important to ensure that the ADC driver has a sufficiently low noise density in the bandwidth of interest. When the MAX11192 is used with its full bandwidth of 50MHz, it is preferable to use an amplifier with an output noise spectral density of less than $6nV\sqrt{Hz}$, to ensure that the overall SNR is not degraded significantly. It is recommended to insert an external RC filter at the ADC input to attenuate out-of-band input noise.
3) To take full advantage of the ADC's excellent dynamic performance, we recommend the use of ADC drivers with equal or even better THD performance. This will ensure that the ADC drivers do not limit distortion performance in the signal path. The ADC drivers listed in Table 1 are all excellent choices.

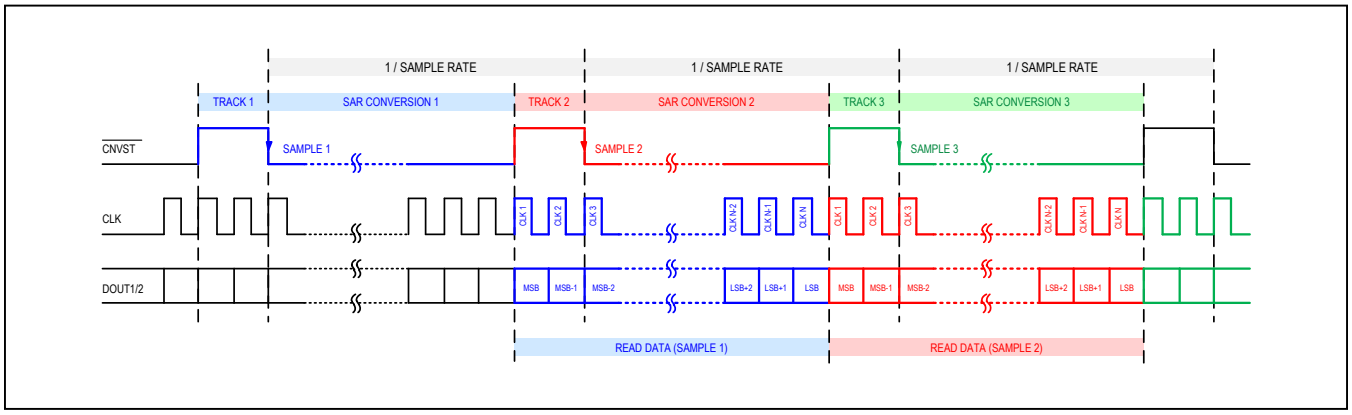


Figure 3. Conversion Timing: Track, SAR Conversion, and Read Operations

Table 1. ADC Driver Amplifier Recommendations

AMPLIFIER	INPUT-NOISE DENSITY (NV/√Hz)	SMALL-SIGNAL BANDWIDTH (MHZ)	SLEW RATE (V/MS)	THD (DB)	ICC (MA)	MAX OFFSET (MV)	COMMENTS
MAX44263	12.7	15	7	-110	0.75	0.05	Low current, low THD at 10kHz
MAX44242	5	10	8	-124	1.2	0.6	High voltage 2.7V to 20V, low THD at 1kHz
MAX9632	1	55	30	-128	3.9	0.125	Low noise, low THD at 10kHz

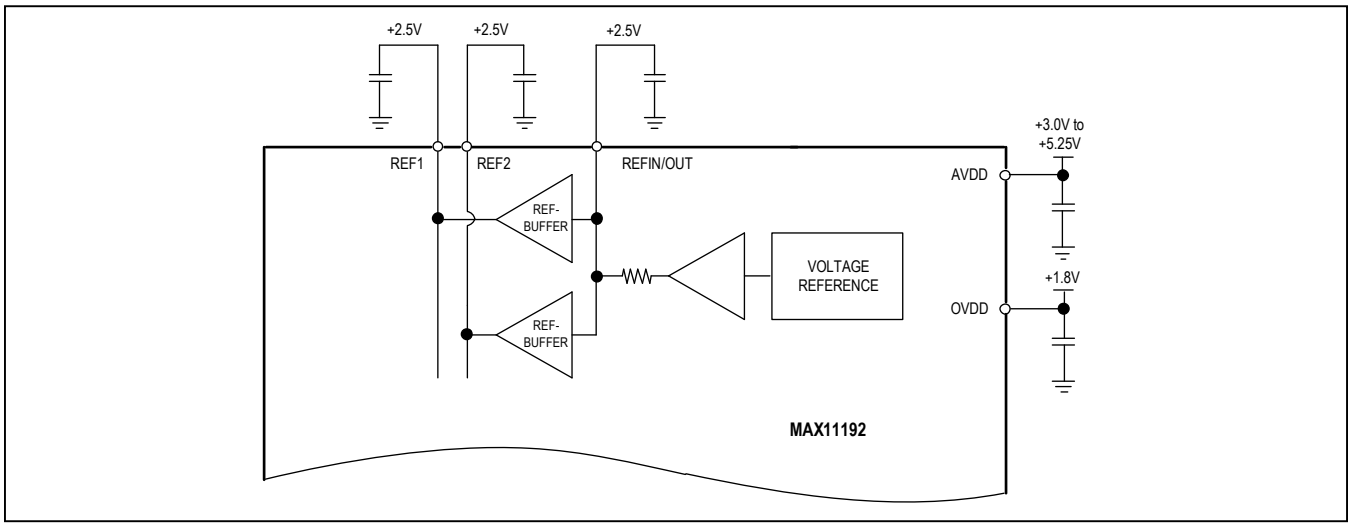


Figure 4. Internal Reference

Input Filtering

Noisy input signals should be filtered prior to the ADC driver amplifier input with an appropriate filter to minimize noise. The RC network shown in the Application Diagram is mainly designed to reduce the load transient seen by the amplifier when the ADC starts the track phase. This network has to satisfy the settling time requirement and provides the benefit of limiting the noise bandwidth.

Voltage Reference Configurations

Using An Internal Reference

The MAX11192 features a 2.5V integrated reference with built-in reference buffers that help to reduce component count and board space. When using internal reference, only bypass capacitors are required on the REF1, REF2, and REFIN/OUT pins (see Figure 4). The REF1/REF2 pins require external bypass capacitors of at least 1µF.

Using An External Reference

To use an external reference (see Figure 5), drive the REFIN/OUT pin directly with an external reference voltage source, ensuring that the reference voltage is no greater than AVDD - 250mV. This will allow the on-chip reference buffers to operate with sufficient supply headroom. The REF1/REF2 pins require external bypass capacitors of at least 1µF.

Table 2 lists excellent choices for low-noise, low-temperature drift external references.

Transfer Function

Figure 6 shows the ideal transfer characteristics for the MAX11192.

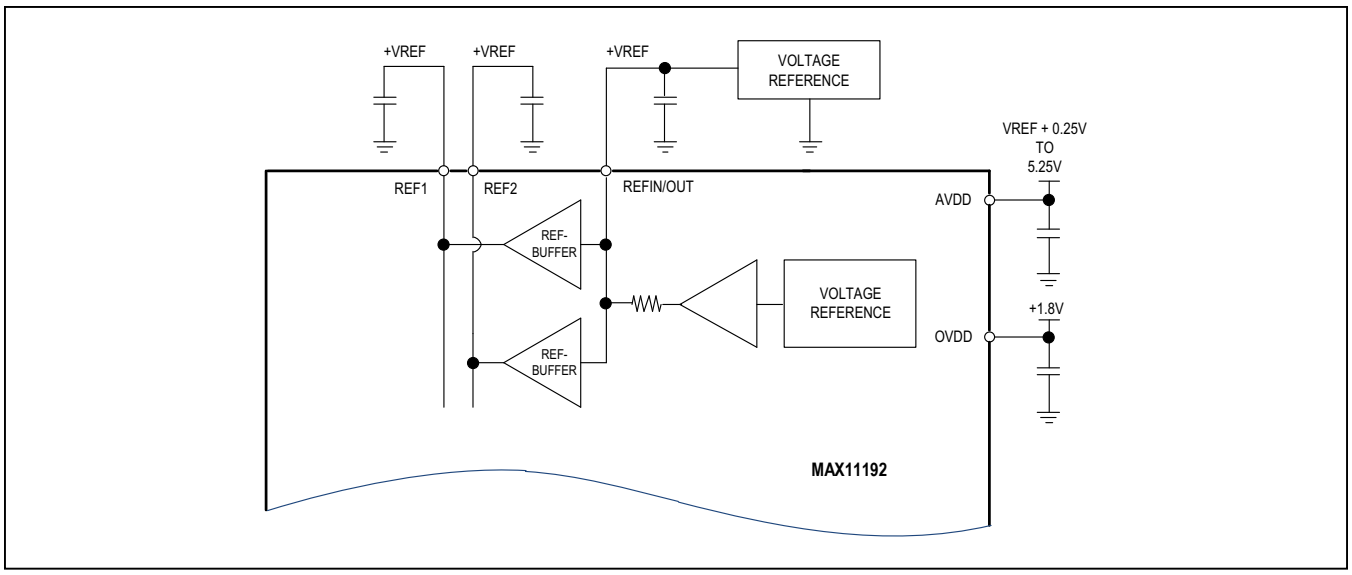


Figure 5. External Reference

Table 2. External Reference Recommendations

REFERENCE	INITIAL ACCURACY (%)	TEMPERATURE DRIFT MAX (PPM/°C)	NOISE (MVP-P)	COMMENTS
MAX6070	±0.04	15	7	Low noise
MAX6133	±0.04	3	16	Very low drift
MAX6072	±0.04	6	9	Dual reference

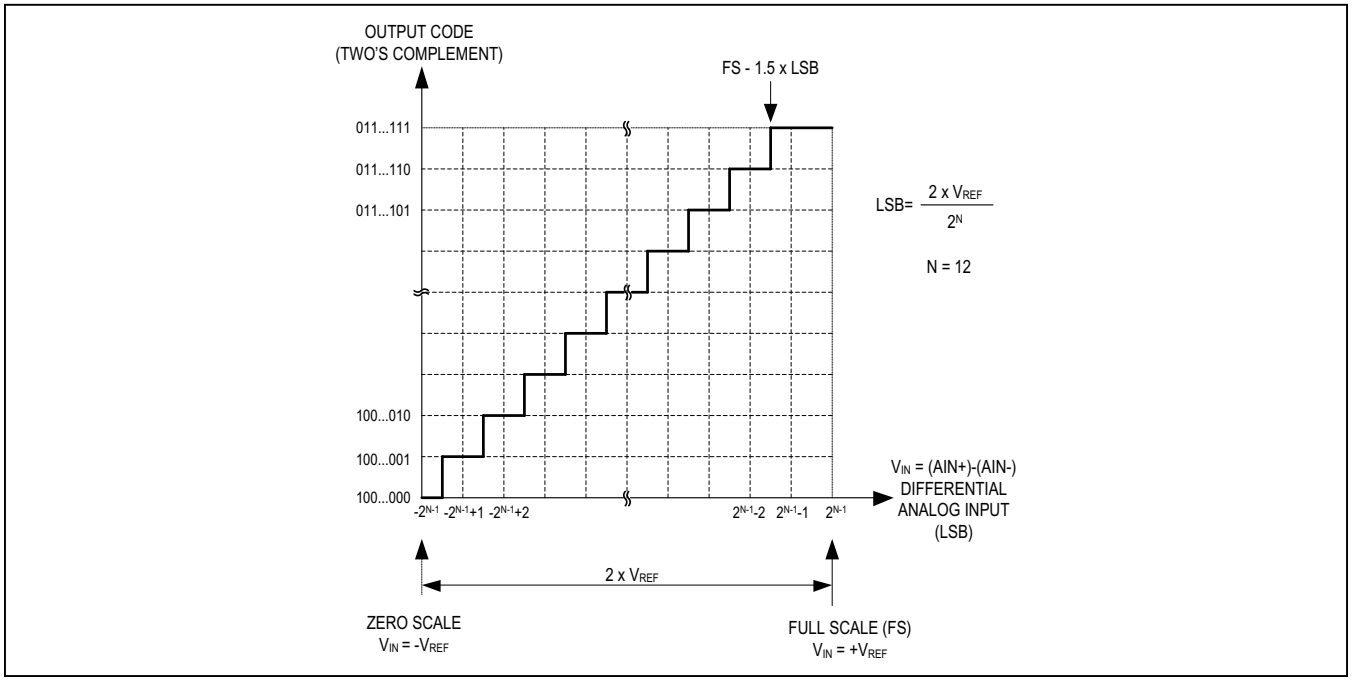


Figure 6. Ideal ADC Transfer Characteristics

Digital Interface

Conversion data may be read in the track phase, the conversion phase, or both. Outlined below are the specifics of the various ways to read conversion data.

The input signals of the two ADC channels are sampled simultaneously on the falling edge of $\overline{CNVST}$ and the conversion is initiated. At the end of the conversion, the ADCs go idle until the next rising edge of $\overline{CNVST}$, at which point the ADCs enter track mode. To complete a conversion, the time between $\overline{CNVST}$ falling and rising edge must be at least the minimum of the conversion time t_{12} (see Figure 11). The conversion data can then be read immediately after the rising edge of the next $\overline{CNVST}$ pulse, which should not occur before the minimum conversion time value (t_{12}) has elapsed. guard against digital noise from the data bus, corrupting the sample.

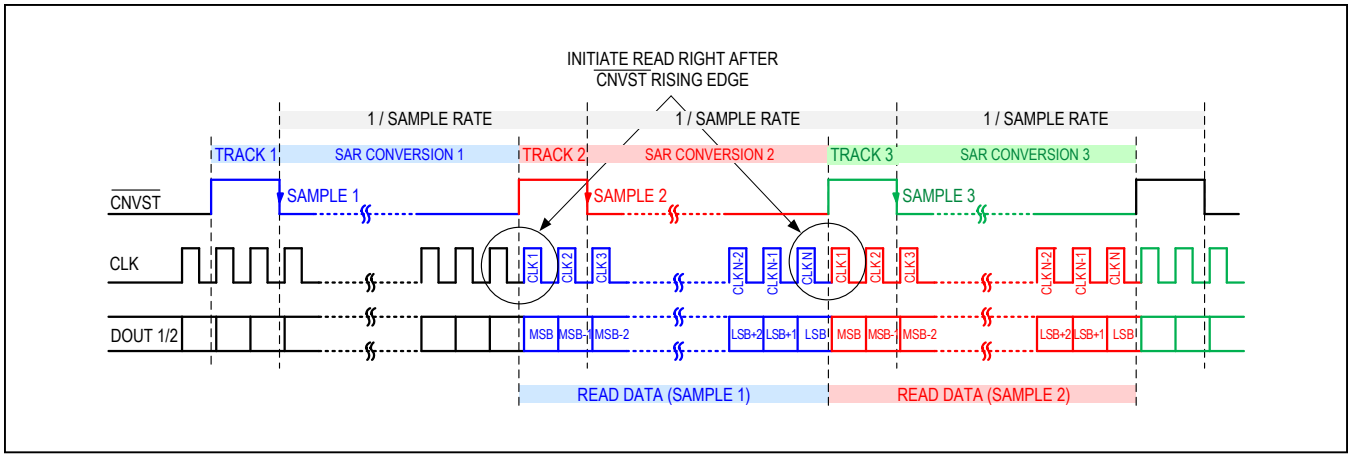


Figure 7. Convert and Data Read MAX11192

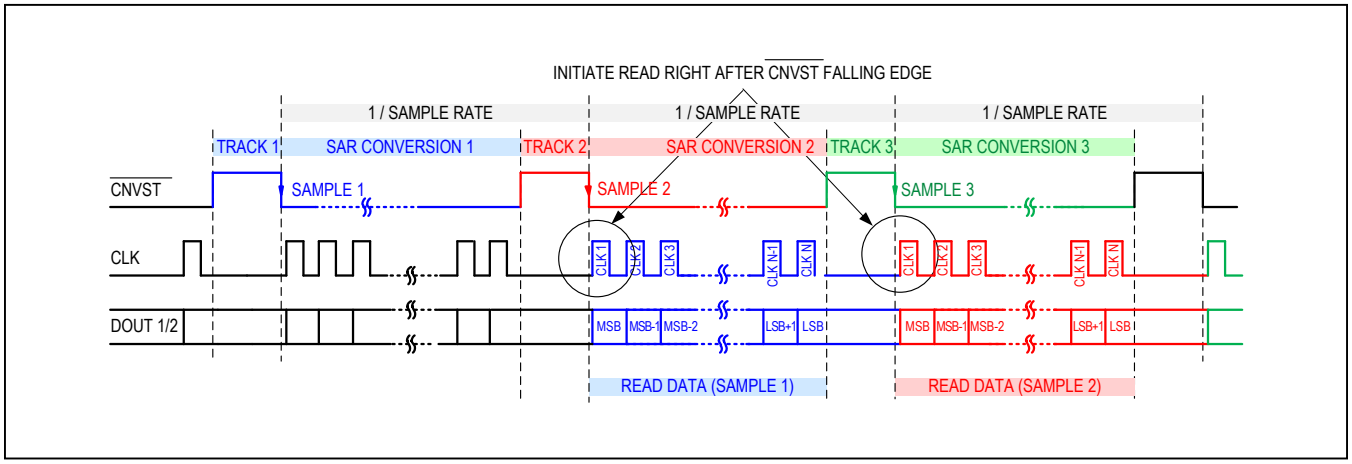


Figure 8. Reading Data After Falling Edge of CNVST

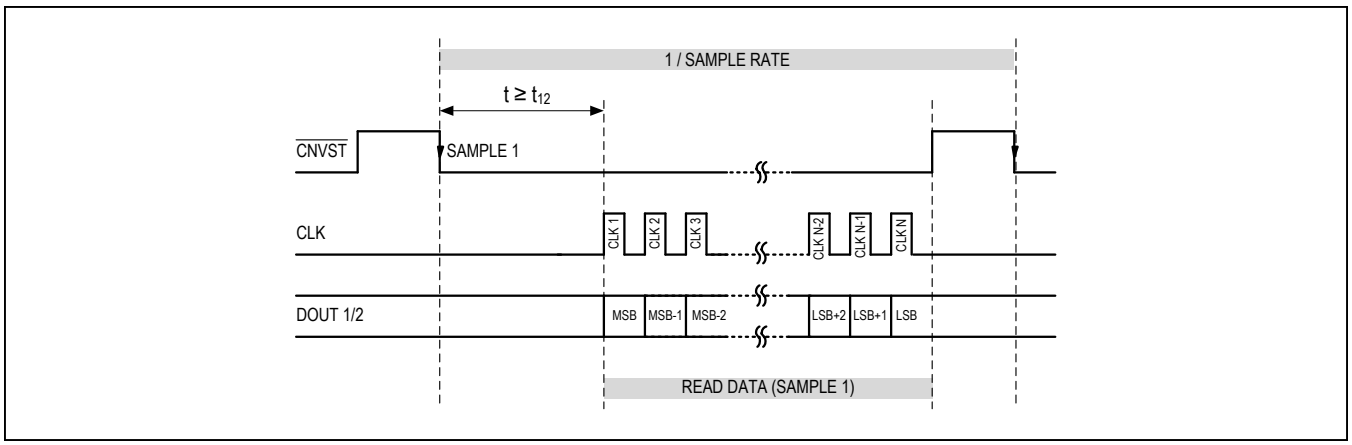


Figure 9. Convert and Data Read in a Single Conversion Period

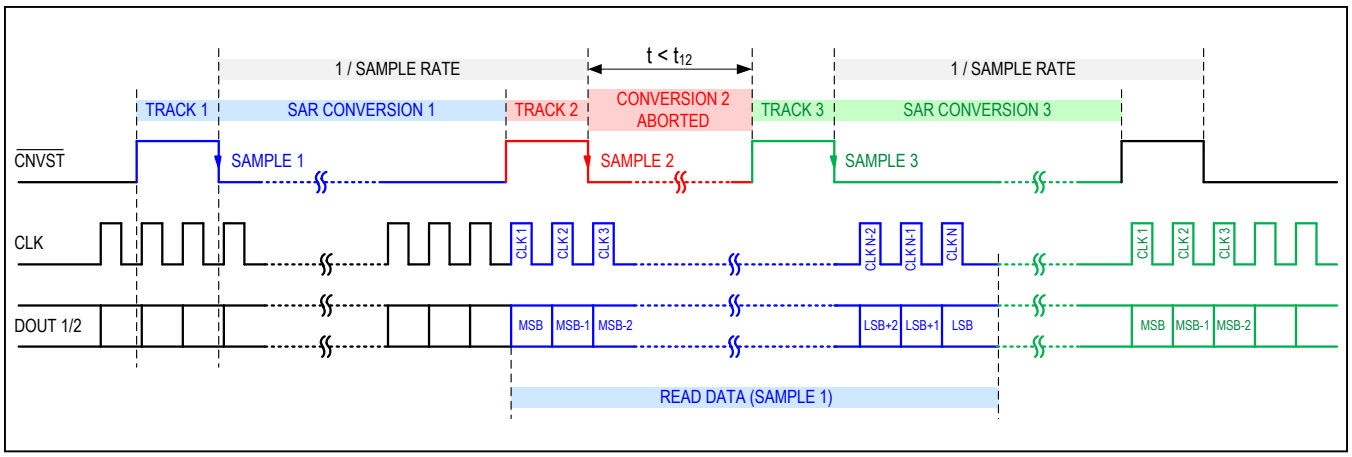


Figure 10. Conversion Abort Data Read

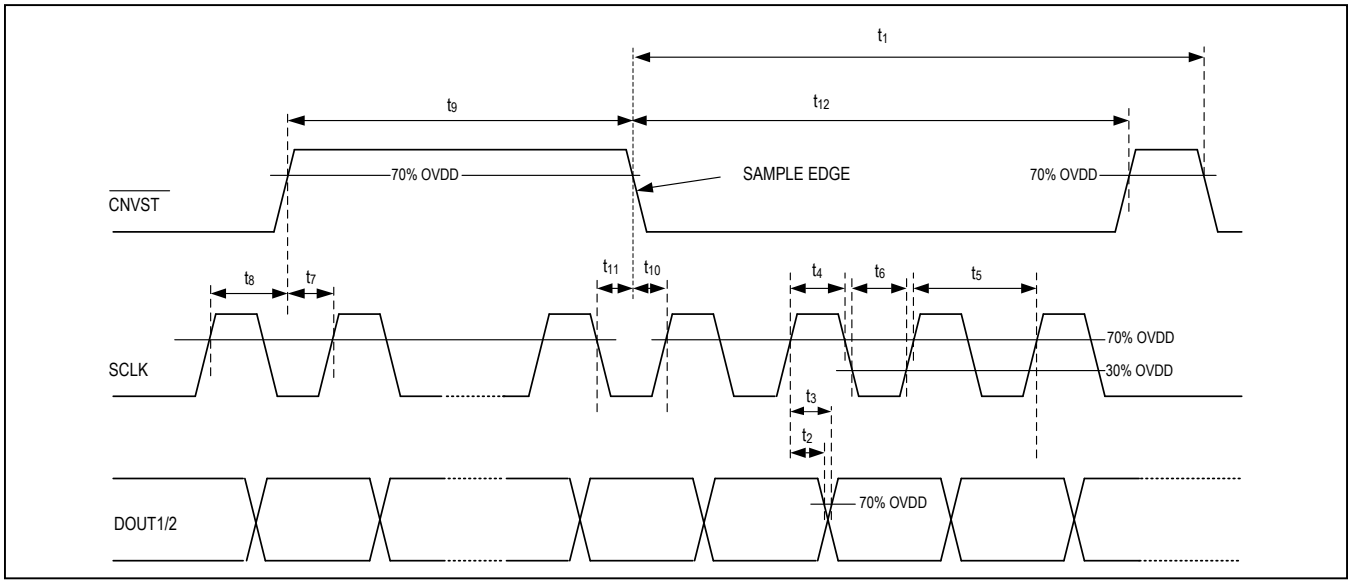


Figure 11. Interface Timing Specifications

Applications Information

Interfacing to Common Input Signals

Real-world signals typically require conditioning before they can be digitized by an ADC. The following outlines common examples of analog signal processing circuits.

The ADCs in the MAX11192 accept differential input signals with unipolar common mode. Refer to THD vs. Input Impedance to use buffers to minimize distortion. The three following examples show input signal conditioning approaches to common signal path configurations.

Differential Unipolar Input

The circuit in Figure 12 shows how amplifiers can be configured to buffer a differential unipolar input signal.

Single-Ended Unipolar Input

The circuit in Figure 13 shows how a single-ended, unipolar signal can interface with the MAX11192. This signal conditioning circuit transforms a 0V to +V_{REF} single-ended input signal to a fully differential output signal with a signal peak-to-peak amplitude of 2 x V_{REF} and common-mode voltage of $V_{REF}/2$. In this case, the single-ended signal source drives the high-impedance input of the first amplifier. This amplifier drives the AIN1+ input, and the second stage amplifier with a peak-to-peak amplitude of V_{REF} and a common-mode output voltage of $V_{REF}/2$. The second amplifier inverts this signal to generate AIN1-, the inverted version of AIN1+.

Single-Ended Bipolar Input

Figure 14 shows a signal conditioning circuit that transforms a -2 x V_{REF} to +2 x V_{REF} single-ended bipolar input signal to a balanced differential output signal with a peak-to-peak amplitude of 2 x V_{REF} and a common-mode voltage $V_{REF}/2$.

The single-ended bipolar input signal drives the inverting input of the first amplifier. This amplifier inverts and adds an offset to the input signal. It also drives the AIN1- input and the second stage amplifier with a peak-to-peak amplitude of V_{REF} and a common-mode output voltage of $V_{REF}/2$. The second amplifier is also in inverting configuration and drives the AIN1+ input. This amplifier adds an offset to generate a signal with a peak-to-peak amplitude of V_{REF} and a common-mode output voltage of $V_{REF}/2$. The input impedance, seen by the signal source, is determined by the input resistor of the first-stage inverting amplifier. The input impedance must be chosen carefully based on the output impedance of the signal source.

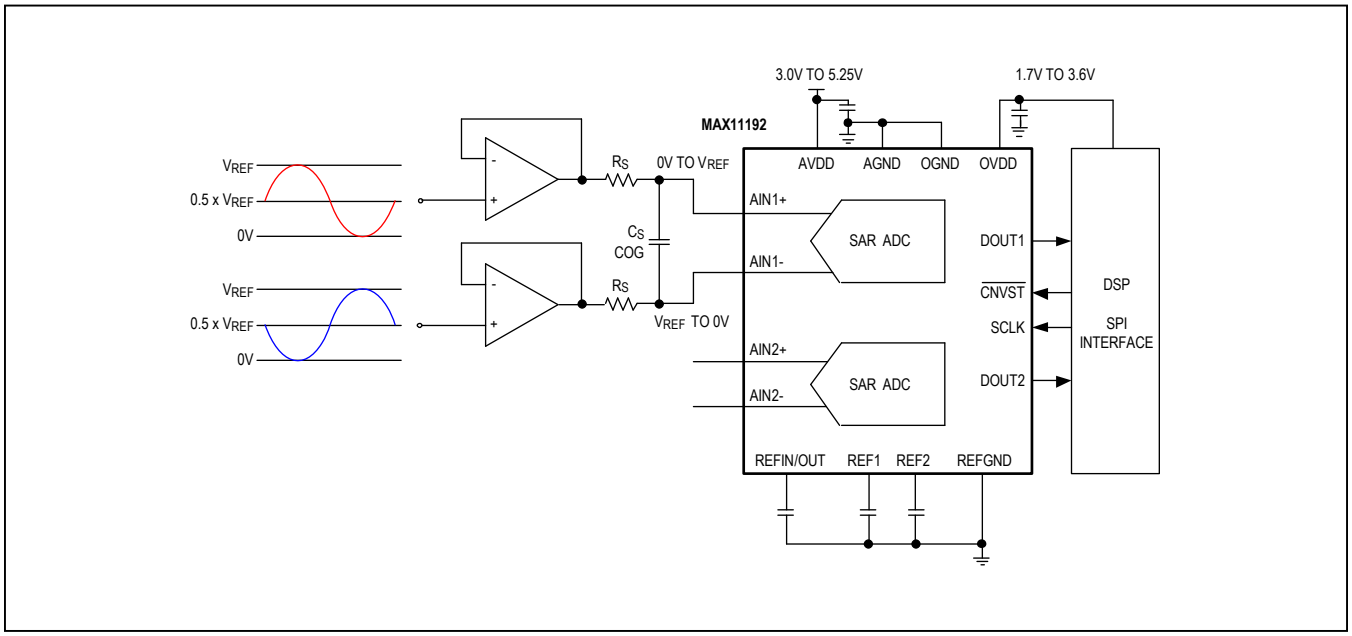


Figure 12. Unipolar Differential Input

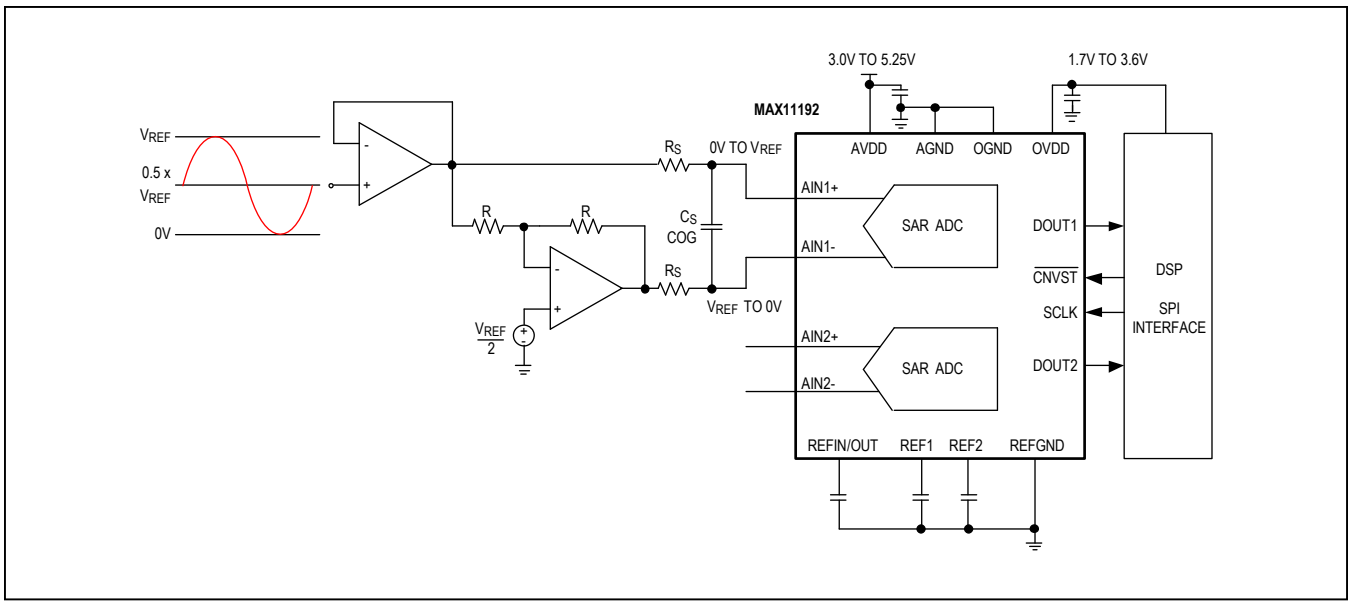


Figure 13. Unipolar Single-Ended Input

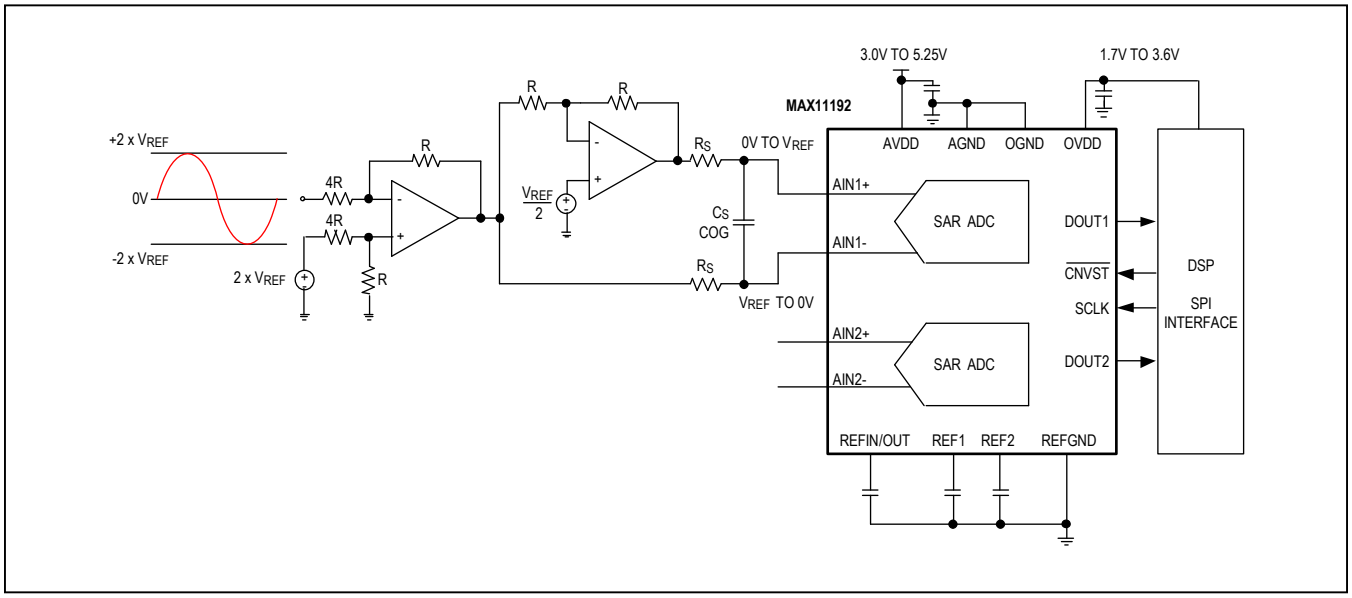


Figure 14. Bipolar Single-Ended Input

Layout, Grounding, and Bypassing

For best performance, use PCBs with ground planes. Ensure that digital and analog signal lines are separated from each other. Do not run analog and digital lines parallel to one another (especially clock lines), and avoid running digital lines underneath the ADC package. A single solid GND plane configuration with digital signals routed from one direction and analog signals from the other provides the best performance. Connect the GND pins of the MAX11192 to this ground plane. Keep the ground return path to the power supply low impedance and as short as possible. A 1nF C0G ceramic chip capacitor should be placed between AINn+ and AINn- as close as possible to the MAX11192. This capacitor reduces the voltage transient seen by the driving stage of the ADC input. For best performance, connect the REF1/2 output to the ground plane with a 16V, 10µF ceramic chip capacitor with a X5R dielectric in a 1210 or smaller case size. Ensure that all bypass capacitors are connected directly into the ground plane with an independent via.

Bypass AVDD and OVDD to the ground plane with 10µF ceramic chip capacitors on each pin as close as possible to the device to minimize parasitic inductance. For best performance, bring the AVDD power plane in from the analog interface side of the MAX11192 and the OVDD power plane from the digital interface side of the device. Figure 15 shows the PCB top layer of a sample layout with optimal placement of passive components.

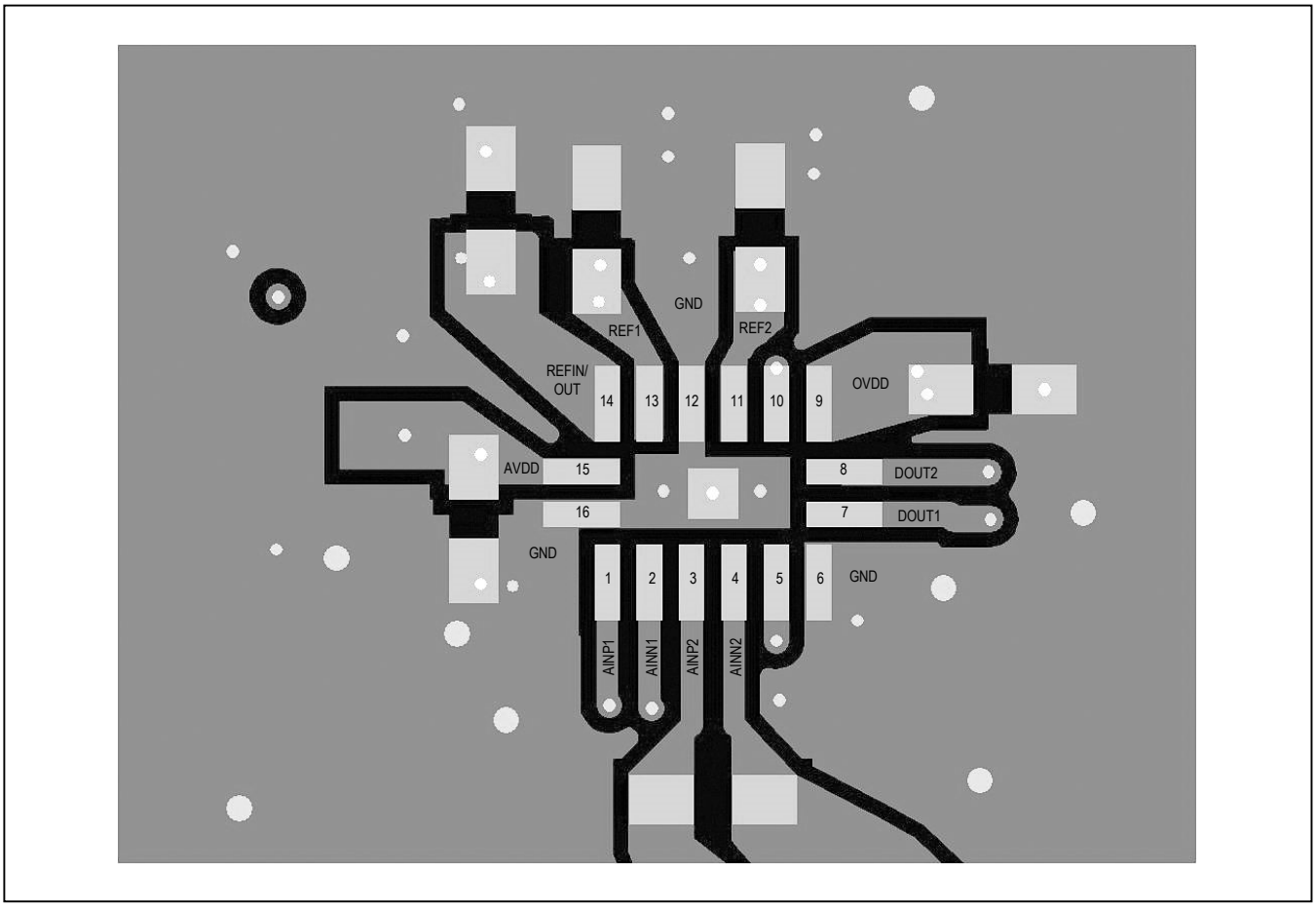


Figure 15. PCB Layout Example for MAX11192

Ordering Information

PART NUMBER	RESOLUTION	TEMP RANGE	PIN-PACKAGE	REFERENCE
MAX11192ATE+	12	-40°C to +125°C	16 UTDFN-EP*	2.5V
MAX11192ATE+T	12	-40°C to +125°C	16 UTDFN-EP*	2.5V

Denotes a lead(Pb)-free/RoHS-compliant package.
T = tape and reel.
**EP = Exposed Pad*

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	4/17	Initial release	—

