



**3.3V SINGLE SUPPLY
OCTAL PECL/TTL-TO-TTL**

**Precision Edge®
SY10H646L
SY100H646L**

FEATURES

- 3.3V power supply
- PECL/TTL-to-TTL version of popular ECLinPS E111AE/LE
- Guaranteed low skew specification
- Three-state enable
- Differential internal design
- VBB output for single-ended operation
- Extra TTL and ECL power/ground pins
- Choice of ECL compatibility: 10K or 100K
- Matched high and low output impedance
- Available in 28-pin PLCC package



Precision Edge®

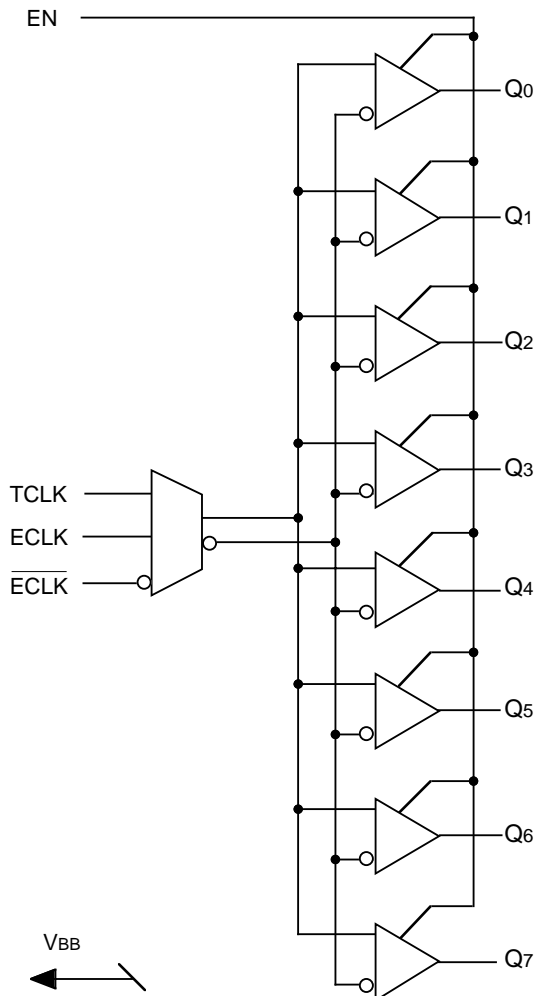
DESCRIPTION

The SY10/100H646L are single supply, low skew translating 1:8 clock drivers. Devices in the Micrel H600 translator series utilize the 28-lead PLCC for optimal power pinning, signal flow-through and electrical performance. The single supply H646L is similar to the HA643 which is a dual supply 1:8 version of the same function.

These devices feature a 24mA TTL output stage, with AC performance specified into a 20pF load capacitance.

The 10H version is compatible with 10K ECL logic levels. The 100H version is compatible with 100K levels.

BLOCK DIAGRAM

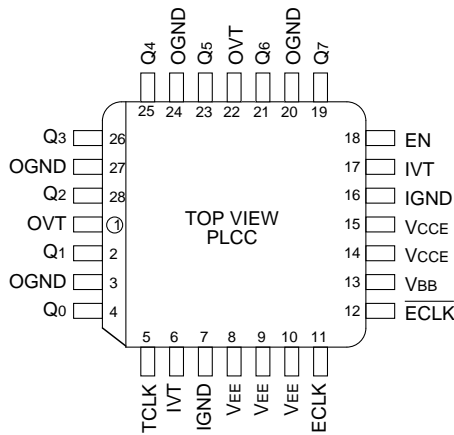


PIN NAMES

Pin	Function
OGND	TTL Output Ground (0V)
OVT	TTL Output Vcc (+3.0V)
IGND	Internal TTL GND (0V)
IVT	Internal TTL Vcc (+3.0V)
VEE	ECL VEE (0V)
VcCE	ECL Ground (+3.0V)
ECLK, $\overline{\text{ECLK}}$	Differential Signal Input (PECL)
VBB	VBB Reference Output
Q0-Q7	Signal Outputs (TTL)
EN	Three-State Enable Input (TTL)
TCLK	Signal Input (TTL)

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PACKAGE/ORDERING INFORMATION



28-Pin PLCC (J28-1)

Ordering Information⁽¹⁾

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY10H646LJC	J28-1	Commercial	SY10H646LJC	Sn-Pb
SY10H646LJCTR ⁽²⁾	J28-1	Commercial	SY10H646LJC	Sn-Pb
SY100H646LJC	J28-1	Commercial	SY100H646LJC	Sn-Pb
SY100H646LJCTR ⁽²⁾	J28-1	Commercial	SY100H646LJC	Sn-Pb
SY10H646LJZ ⁽³⁾	J28-1	Commercial	SY10H646LJZ with Pb-Free bar-line indicator	Matte-Sn
SY10H646LJZTR ^(2, 3)	J28-1	Commercial	SY10H646LJZ with Pb-Free bar-line indicator	Matte-Sn
SY100H646LJZ ⁽³⁾	J28-1	Commercial	SY100H646LJZ with Pb-Free bar-line indicator	Matte-Sn
SY100H646LJZTR ^(2, 3)	J28-1	Commercial	SY100H646LJZ with Pb-Free bar-line indicator	Matte-Sn

Notes:

1. Contact factory for die availability. Dice are guaranteed at T_A = 25°C, DC Electricals only.
2. Tape and Reel.
3. Pb-Free package is recommended for new designs.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Rating	Value	Unit
VE (ECL) VT (TTL)	Power Supply Voltage	-0.5 to +7.0 -0.5 to +7.0	V
VI (ECL) VI (TTL)	Input Voltage	0.0 to VEE -0.5 to VCC	V
VOUT (TTL)	Disabled 3-State Output	0.0 to VCCT	V
IOUT (ECL)	Output Current - Continuous - Surge	50 100	mA
TLEAD	Lead Temperature Range (soldering, 20sec)	+260	°C
Tstore	Storage Temperature	-65 to +150	°C
TA	Operating Temperature	0 to +85	°C

Note:

- Do not exceed.

TRUTH TABLE

TCLK	ECLK	$\overline{\text{ECLK}}$	EN	Q
GND	L	H	H	L
GND	H	L	H	H
H	GND	GND	H	H
L	GND	GND	H	L
X	X	X	L	Z

Note:

- X = Don't Care
- L = Low Voltage Level
- H = High Voltage Level
- Z = Three-State

DC ELECTRICAL CHARACTERISTICS

OVT = IVT = VCCE = 3.0V to 3.6V

Symbol	Parameter	TA = 0°C		TA = +25°C		TA = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
ICCL	Power Supply Current	—	120	—	120	—	120	mA	Total all OVT, IVT, and VCCE pins
ICCH		—	120	—	120	—	120		

TTL DC ELECTRICAL CHARACTERISTICS

OVT = IVT = VCCE = 3.0V to 3.6V

Symbol	Parameter	TA = 0°C		TA = +25°C		TA = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
VIH	Input HIGH Voltage	2.0	—	2.0	—	2.0	—	V	
VIL	Input LOW Voltage	—	0.8	—	0.8	—	0.8	V	
IiH	Input HIGH Current	—	20 100	—	20 100	—	20 100	μA	VIN = 2.7 V VIN = VCC
IiL	Input LOW Current	—	-0.4	—	-0.4	—	-0.4	mA	VIN = 0.5 V
VOH	Output HIGH Voltage	2.0	—	2.0	—	2.0	—	V	IOH = -3.0 mA
VOL	Output LOW Voltage	—	0.5	—	0.5	—	0.5	V	IoL = 24 mA
VIK	Input Clamp Voltage	—	-1.2	—	-1.2	—	-1.2	V	IIN = -18mA
Ios	Output Short Circuit Current	-100	—	-100	—	-100	—	mA	VOH = 0V

10H ECL DC ELECTRICAL CHARACTERISTICS

OVT = IVT = VCCE = 3.0V to 3.6V

Symbol	Parameter	TA = 0°C		TA = +25°C		TA = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
I _{IH}	Input HIGH Current	—	225	—	175	—	175	μA	—
I _{IL}	Input LOW Current	0.5	—	0.5	—	0.5	—	μA	—
V _{IH}	Input HIGH Voltage ⁽¹⁾	2.130	2.460	2.170	2.490	2.240	2.580	V	V _E = 3.3V
V _{IL}	Input LOW Voltage ⁽¹⁾	1.350	1.820	1.350	1.820	1.350	1.855	V	V _E = 3.3V
V _{BB}	Output Reference Voltage ⁽¹⁾	1.920	2.030	1.950	2.050	1.990	2.110	V	V _E = 3.3V

Note:1. V_{IH}, V_{IL} and V_{BB} are referenced to V_{CC} and will vary 1:1 with the power supply. The levels shown are for V_{CC} = +3.3V.**100H ECL DC ELECTRICAL CHARACTERISTICS**

OVT = IVT = VCCE = 3.0V to 3.6V

Symbol	Parameter	TA = 0°C		TA = +25°C		TA = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
I _{IH}	Input HIGH Current	—	225	—	175	—	175	μA	—
I _{IL}	Input LOW Current	0.5	—	0.5	—	0.5	—	μA	—
V _{IH}	Input HIGH Voltage ⁽¹⁾	2.135	2.420	2.135	2.420	2.135	2.420	V	V _E = 3.3V
V _{IL}	Input LOW Voltage ⁽¹⁾	1.490	1.825	1.490	1.825	1.490	1.825	V	V _E = 3.3V
V _{BB}	Output Reference Voltage ⁽¹⁾	1.920	2.040	1.920	2.040	1.920	2.040	V	V _E = 3.3V

Note:1. V_{IH}, V_{IL} and V_{BB} are referenced to V_{CC} and will vary 1:1 with the power supply. The levels shown are for V_{CC} = +3.3V.

AC ELECTRICAL CHARACTERISTICS

IVT = OVT = VCCE = 3.0V to 3.6V

Symbol	Parameter	TA = 0°C			TA = +25°C			TA = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
tPLH	Propagation Delay ECLK to Q	2.3	—	3.3	2.25	—	3.25	2.2	—	3.2	ns	CL = 20pF
tPHL	TCLK to Q	2.3	—	3.3	2.25	—	3.25	2.2	—	3.2		
tskpp	Part-to-Part Skew ^(1,4)	—	—	0.5	—	—	0.5	—	—	0.5	ns	CL = 20pF
tskew++	Within-Device Skew ^(2,4)	—	—	0.3	—	—	0.3	—	—	0.3	ns	CL = 20pF
tskew--	Within-Device Skew ^(3,4)	—	—	0.3	—	—	0.3	—	—	0.3	ns	CL = 20pF
tr	Rise 0.8V to 2.0V	0.3	—	1.5	0.3	—	1.5	0.3	—	1.5	ns	CL = 20pF
tf	Fall Time 0.8V to 2.0V	0.3	—	1.5	0.3	—	1.5	0.3	—	1.5	ns	CL = 20pF
tPW	Output Pulse Width										ns	CL = 20pF
	66MHz @ 2.0V	5.5	—	—	5.5	—	—	5.5	—	—		
	66MHz @ 0.8V	5.5	—	—	5.5	—	—	5.5	—	—		
	60MHz @ 2.0V	6.0	—	—	6.0	—	—	6.0	—	—		
	60MHz @ 0.8V	6.0	—	—	6.0	—	—	6.0	—	—		
tStability	Clock Stability ⁽⁷⁾	—	—	±75	—	—	±75	—	—	±75	ps	CL = 20pF
fMAX	Maximum Input Frequency ^(5,6)	160	—	—	160	—	—	160	—	—	MHz	CL = 20pF

Notes:

1. Device-to-Device Skew considering HIGH-to-HIGH or LOW-to-LOW transitions at common Vcc level.
2. Within-Device Skew considering HIGH-to-HIGH transitions at common Vcc level.
3. Within-Device Skew considering LOW-to-LOW transitions at common Vcc level.
4. All skew parameters are guaranteed but not tested.
5. Frequency at which output levels will meet a 0.8V to 2.0V minimum swing.
6. The fMAX value is specified as the minimum guaranteed maximum frequency. Actual operational maximum frequency may be greater.
7. Clock stability is the period variation between two successive rising edges.

ADDITIONAL INFORMATION

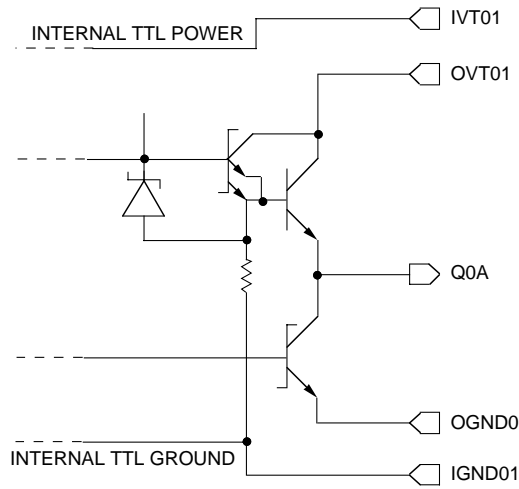


Figure 1. Output Structure

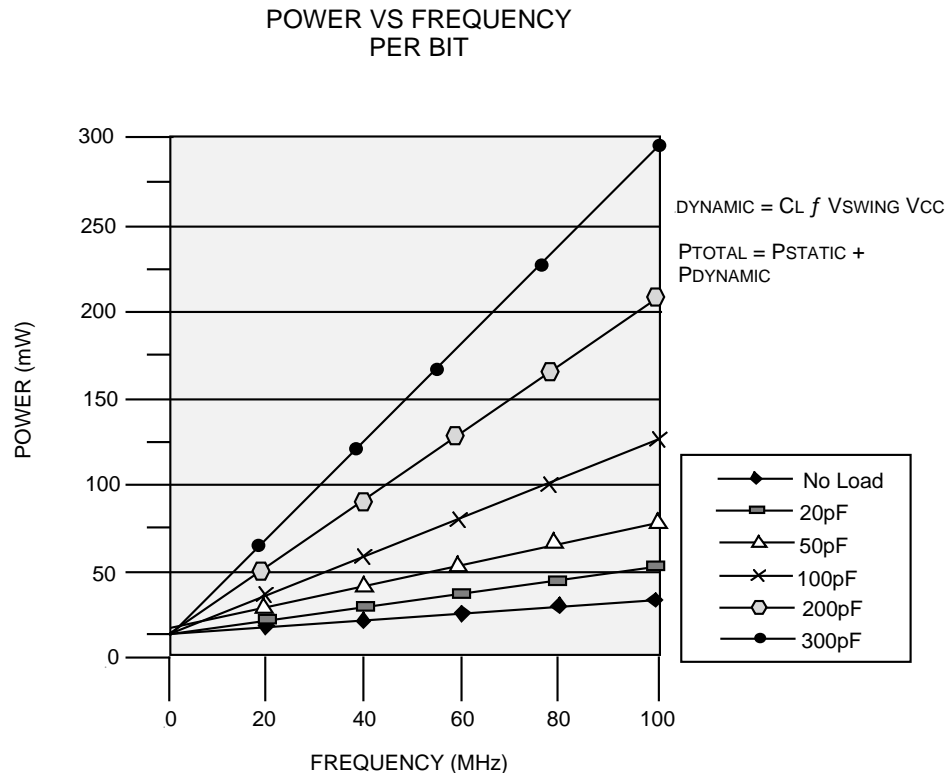
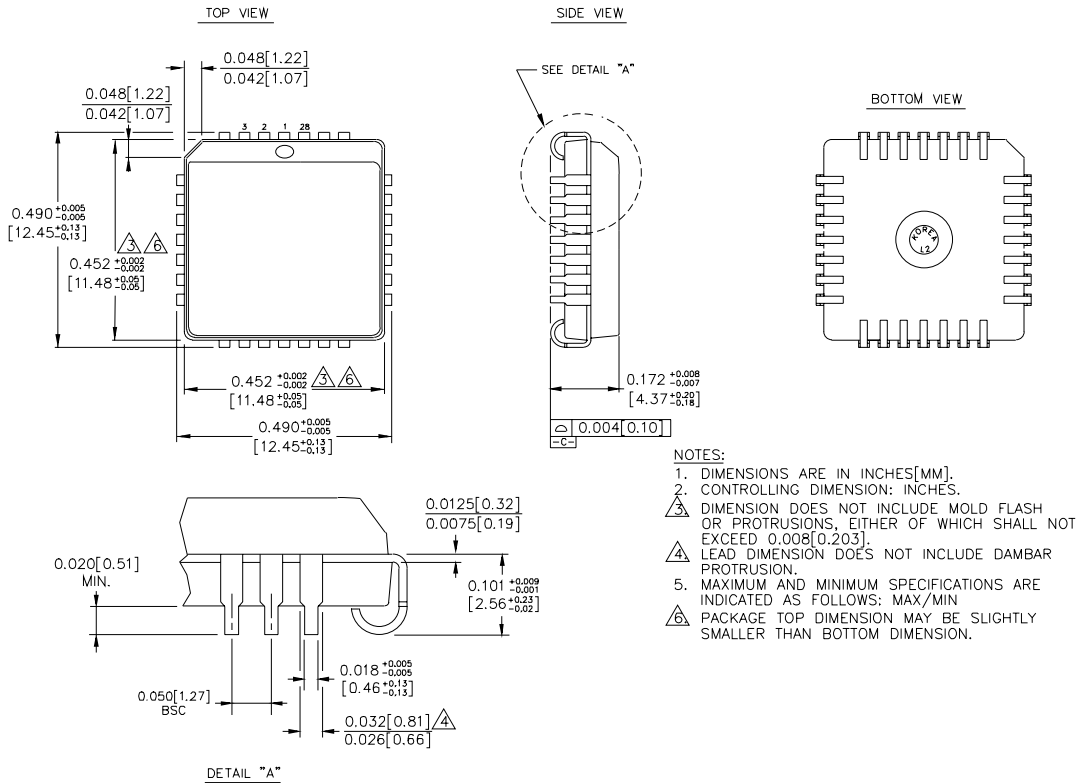


Figure 2. Power Versus Frequency (Typical)

28-PIN PLCC (J28-1)



Rev. 03

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