PIC16(L)F15313/23

PIC16(L)F15313/23 Family
Silicon Errata and Data Sheet Clarification

The PIC16(L)F15313/23 family devices that you have received conform functionally to the current Device Data Sheet (DS40001897**A**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC16(L)F15313/23 silicon.

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**A3**).

Data Sheet clarifications and corrections start on page 4, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate website (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB IDE project.
3. Configure the MPLAB IDE project for the appropriate device and hardware debugger.
4. Based on the version of MPLAB IDE you are using, do one of the following:
   a) For MPLAB IDE 8, select *Programmer > Reconnect*.
   b) For MPLAB X IDE, select *Window > Dashboard* and click the **Refresh Debug Tool Status** icon ( ).
5. Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note:	If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC16(L)F15313/23 silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID(1)	Revision ID for Silicon Revision(2)	
		A2	A3
PIC16F15313	30BEh	2002h	2003h
PIC16LF15313	30BFh	2002h	2003h
PIC16F15323	30C0h	2002h	2003h
PIC16LF15323	30C1h	2002h	2003h

Note 1: The Device IDs (DEVID and DEVREV) are located at addresses 8006h and 8005h, respectively. They are shown in hexadecimal in the format "DEVID DEVREV".

2: Refer to the *"PIC16(L)F153XX Memory Programming Specification"* (DS40001838) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions	
				A2	A3
Electrical Specifications	SMBus 2.0	1.1	The maximum V_{IL} level changes when V_{DD} is below 4.0V at 125°C.	X	—
	Fixed Voltage Reference (FVR) Accuracy	1.2	Fixed Voltage Reference (FVR) output tolerance may be higher than specified at temperatures below –20°C.	X	—
Comparator	Input Pin	2.1	Negative Input Pin on RA4 is not functional.	X	—
I/O Port	SMBus 2.0	3.1	SMBus 2.0 levels are not functional on the default I^2C function pins for SCL and SDA.	X	—
	I^2C Driver	3.2	I^2C levels are not functional on the default I^2C function pins for SCL and SDA.	X	—

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A3**).

1. Module: Electrical Specifications

1.1 SMBus 2.0 V_{IL} Level

At 125°C when the V_{DD} voltage level supplied to the device is 4.0V and above, the maximum SMBus 2.0 voltage level for the V_{IL} parameter is 0.8V. When V_{DD} drops below 4.0V, the maximum SMBus voltage level for V_{IL} drops to 0.7V. This issue applies to extended temperature devices only.

Work around

None.

Affected Silicon Revisions

A2	A3						
X							

1.2 Fixed Voltage Reference (FVR) Accuracy

At temperatures below -20°C, the output voltage for the FVR may be greater than the levels specified in the data sheet. This will apply to all three gain amplifier settings, (1X, 2X, 4X). The affected parameter numbers found in the data sheet are: FVR01 (1X gain setting), FVR02 (2X gain setting), and FVR03 (4X gain setting).

Work around

None.

Affected Silicon Revisions

A2	A3						
X							

2. Module: Comparator

2.1 Input Pin

The negative input pin for the C1 Comparator, on RA4, is not functional on the PIC16(L)F15313 devices.

Work around

Use another negative input pin for the C1 comparator.

Affected Silicon Revisions

A2	A3						
X							

3. Module: I/O Port

3.1 SMBus 2.0

The SMBus 2.0 signal levels are not available on the default I^2C function pins on PORTA for SCL and SDA on the PIC16(L)F15313. Standard ST and TTL levels are still available for these pins, which are configurable through the INLVLA register settings.

Work around

None.

Affected Silicon Revisions

A2	A3						
X							

3.2 I^2C Drivers

The I^2C signal levels are not available on the default I^2C function pins on PORTA for SCL and SDA on the PIC16(L)F15313. Standard ST and TTL levels are still available for these pins, which are configurable through the INLVLA register settings.

Work around

None.

Affected Silicon Revisions

A2	A3						
X							

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS40001897**A**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

None.

APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (4/2017)

Initial release of this document.

Rev B Document (8/2017)

Added Affected Silicon Revision A3. Other minor corrections.

Note the following details of the code protection feature on Microchip devices:

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