3.3V Low Skew 1-to-4
LVTTL/LVCMOS to LVPECL Fanout Buffer

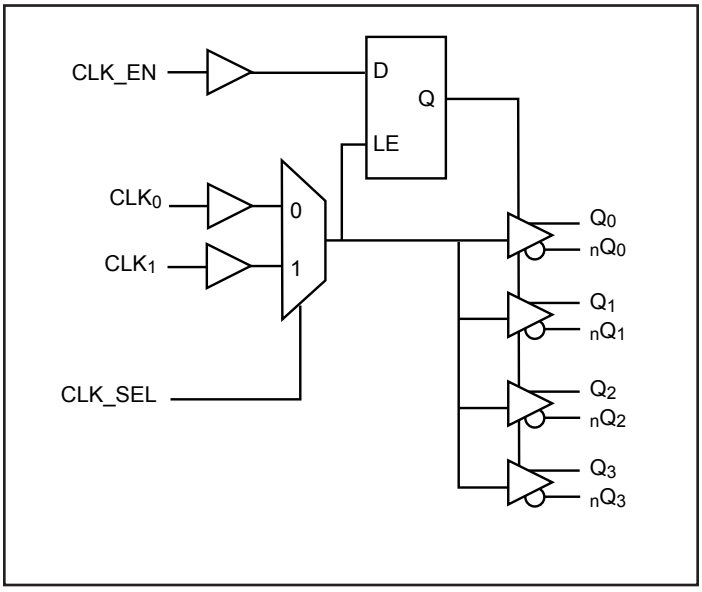
Features

- Maximum operation frequency: 500 MHz
- 4 pair of differential LVPECL outputs
- Selectable CLK_0 and CLK_1 inputs
- CLK_0, CLK_1 accept LVCMOS, LVTTL input level
- Output Skew: 40ps (typical)
- Propagation delay: 1.5ns (typical)
- 3.3V power supply
- Additive jitter of 0.03ps (typical)
- Operating Temperature: -40°C to 85°C
- Packaging (Pb-free & Green available):
  — 20-pin TSSOP (L)

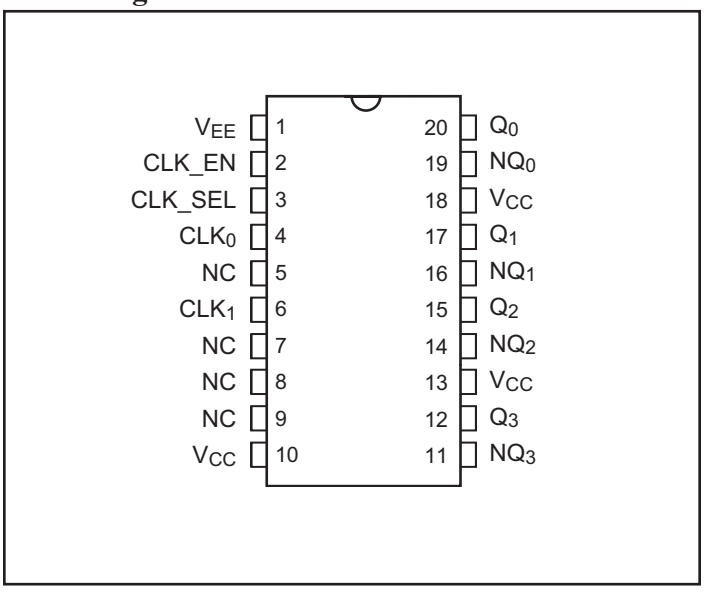
Description

The PI6C48535-01B is a high-performance low-skew LVPECL fanout buffer. PI6C48535-01B features two selectable single-ended clock inputs and translates to four LVPECL outputs. The CLK_0 and CLK_1 inputs accept LVCMOS or LVTTL signals. The outputs are synchronized with input clock during asynchronous assertion/deassertion of CLK_EN pin. PI6C48535-01B is ideal for single-ended LVTTL/LVCMOS to LVPECL translations. Typical clock translation and distribution applications are data-communications and telecommunications.

Block Diagram



Pin Configuration



Pin Description

Name	Pin #	Type	Description
V_{EE}	1	P	Connect to Negative power supply
CLK_EN	2	I_PU	Synchronizing clock enable. When high, clock outputs follow clock input. When low, Qx outputs are forced low, nQx outputs are forced high. LVCMOS/LVTTL level with 50KΩ pull up.
CLK_SEL	3	I_PD	Clock select input. When high, selects CLK_1 input. When low, selects CLK_0 input. LVCMOS/LVTTL level with 50KΩ pull down.
CLK_0	4	I_PD	LVCMOS / LVTTL clock input
CLK_1	6	I_PD	LVCMOS / LVTTL clock input
NC	5, 7, 8, 9		No internal connection.
V_{CC}	10, 13, 18	P	Connect to 3.3V.
Q_3, $_nQ_3$	11, 12	O	Differential output pair, LVPECL interface level.
Q_2, $_nQ_2$	14, 15	O	Differential output pair, LVPECL interface level.
Q_1, $_nQ_1$	16, 17	O	Differential output pair, LVPECL interface level.
Q_0, $_nQ_0$	19, 20	O	Differential output pair, LVPECL interface level.

Notes:
1. I = Input, O = Output, P = Power supply connection, I_PD = Input with pull down, I_PU = Input with pull up.

Pin Characteristics

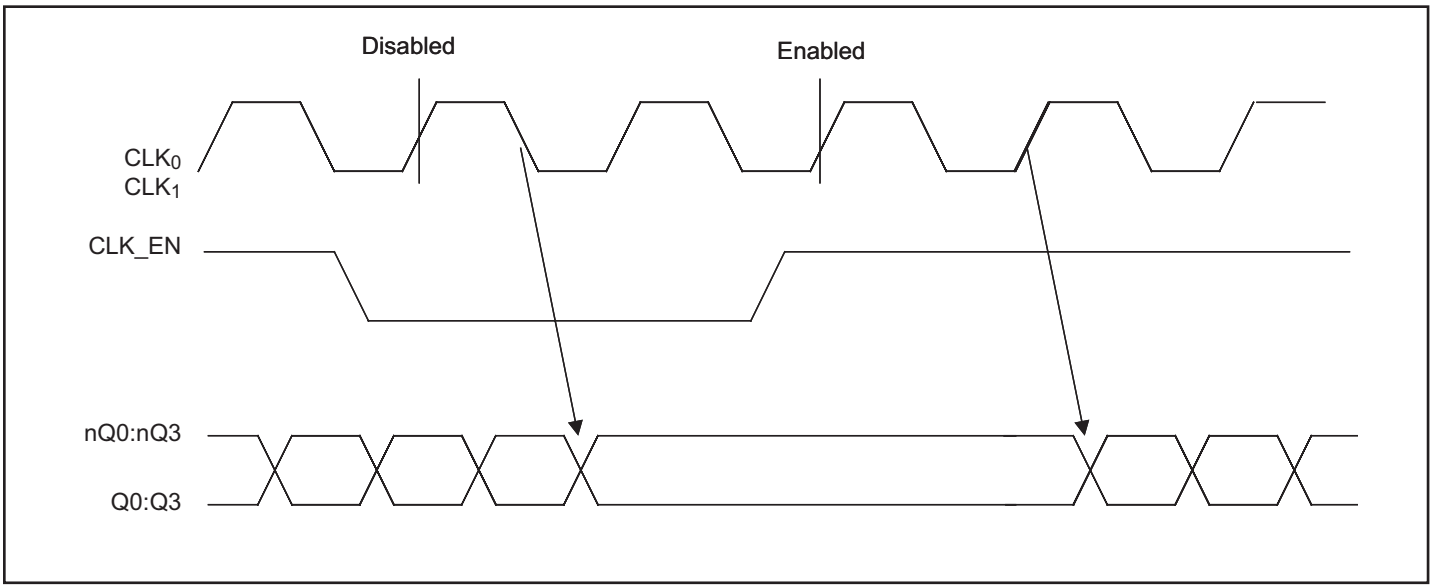
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
C_{IN}	Input Capacitance				4	pF
R_pullup	Input Pullup Resistance			50		KΩ
R_pulldown	Input Pulldown Resistance			50		

Control Input Function Table

Inputs			Outputs	
CLK_EN	**CLK_SEL**	**Selected Source**	**Q_0:Q_3**	**$_nQ_0$:$_nQ_3$**
0	0	CLK_0	Diasbled: Low	Diasbled: High
0	1	CLK_1	Disabled: Low	Disabled: High
1	0	CLK_0	Enabled	Enabled
1	1	CLK_1	Enabled	Enabled

Notes:
1. After CLK_EN switches, the clock outputs are disabled or enabled following a rising and falling input clock edge as show below.

Figure 1. CLK_EN Timing Diagram



Clock Input Function Table

Inputs	Outputs	
CLK_0 or CLK_1	Q_0:Q_3	${}_nQ_0$:${}_nQ_3$
0	LOW	HIGH
1	HIGH	LOW

Absolute Maximum Ratings

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{CC}	Supply voltage	Referenced to GND			4.6	V
V_{IN}	Input voltage	Referenced to GND	-0.5		V_{CC}+0.5V	
V_{OUT}	Output voltage	Referenced to GND	-0.5		V_{CC}+0.5V	
T_{STG}	Storage temperature		-65		150	°C

Notes:
1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress speci fications only and correct functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Operating Conditions

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{CC}	Power Supply Voltage		3.0	3.3	3.6	V
T_A	Ambient Temperature		-40		85	°C
I_{DD}	Power Supply Current	All outputs unloaded			130	mA

LVCMOS/LVTTL DC Characteristics (T_A = -40°C to 85°C, V_{CC} = 3.0V to 3.6V unless otherwise stated below.)

Symbol	Parameter		Conditions	Min.	Typ.	Max.	Units
V_{IH}	Input High Voltage	CLK_0, CLK_1, CLK_EN, CLK_SEL		2		V_{CC}+0.3	V
V_{IL}	Input Low Voltage	CLK_0, CLK_1		-0.3		0.8	V
		CLK_EN, CLK_SEL		-0.3		0.8	V
I_{IH}	Input High Current	CLK0, CLK1, CLK_SEL	$V_{IN} = V_{CC}$ = 3.6V			150	uA
		CLK_EN	$V_{IN} = V_{CC}$ = 3.6V			15	uA
I_{IL}	Input Low Current	CLK_0, CLK_1, CLK_SEL	V_{IN} = 0V, V_{CC} = 3.6V	-10			uA
		CLK_EN	V_{IN} = 0V, V_{CC} = 3.6V	-150			uA

LVPECL DC Characteristics

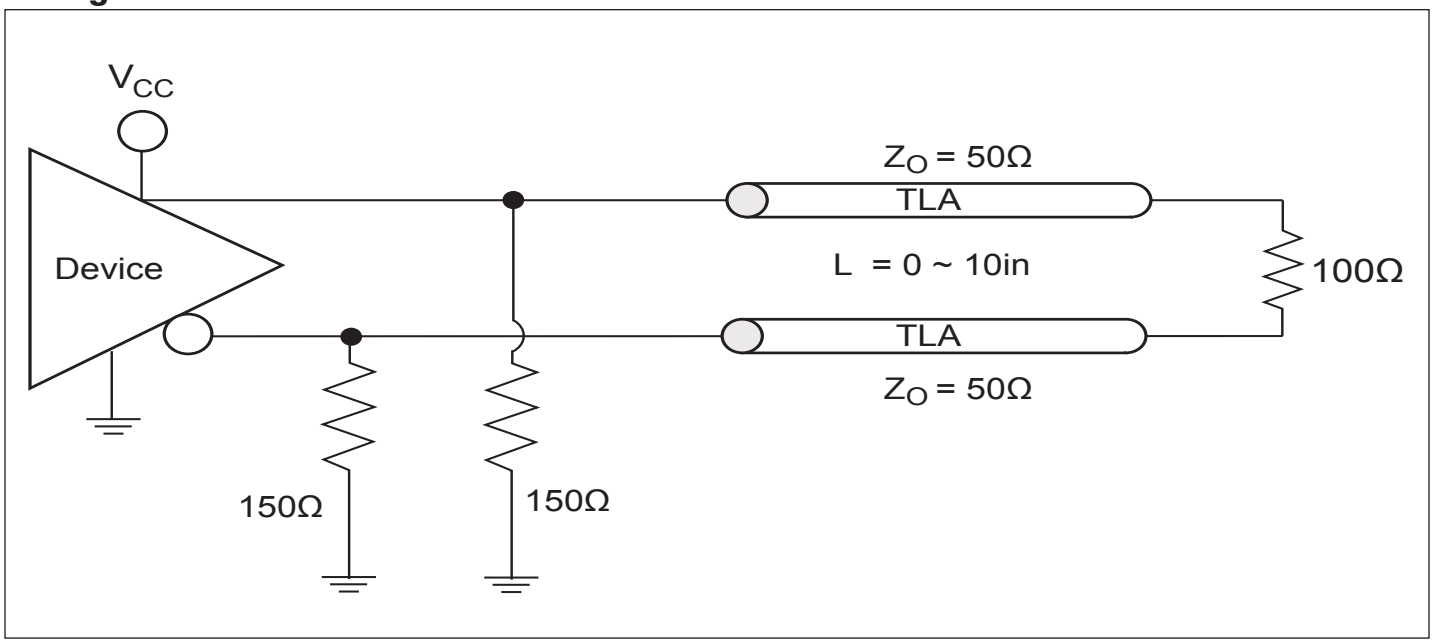
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{OH}	Output High Voltage	V_{CC} = 3.3V	2.1		2.6	V
V_{OL}	Output Low Voltage	V_{CC} = 3.3V	1.3		1.8	

AC Characteristics (T_A = -40°C to 85°C, V_{CC} = 3.0V to 3.6V)

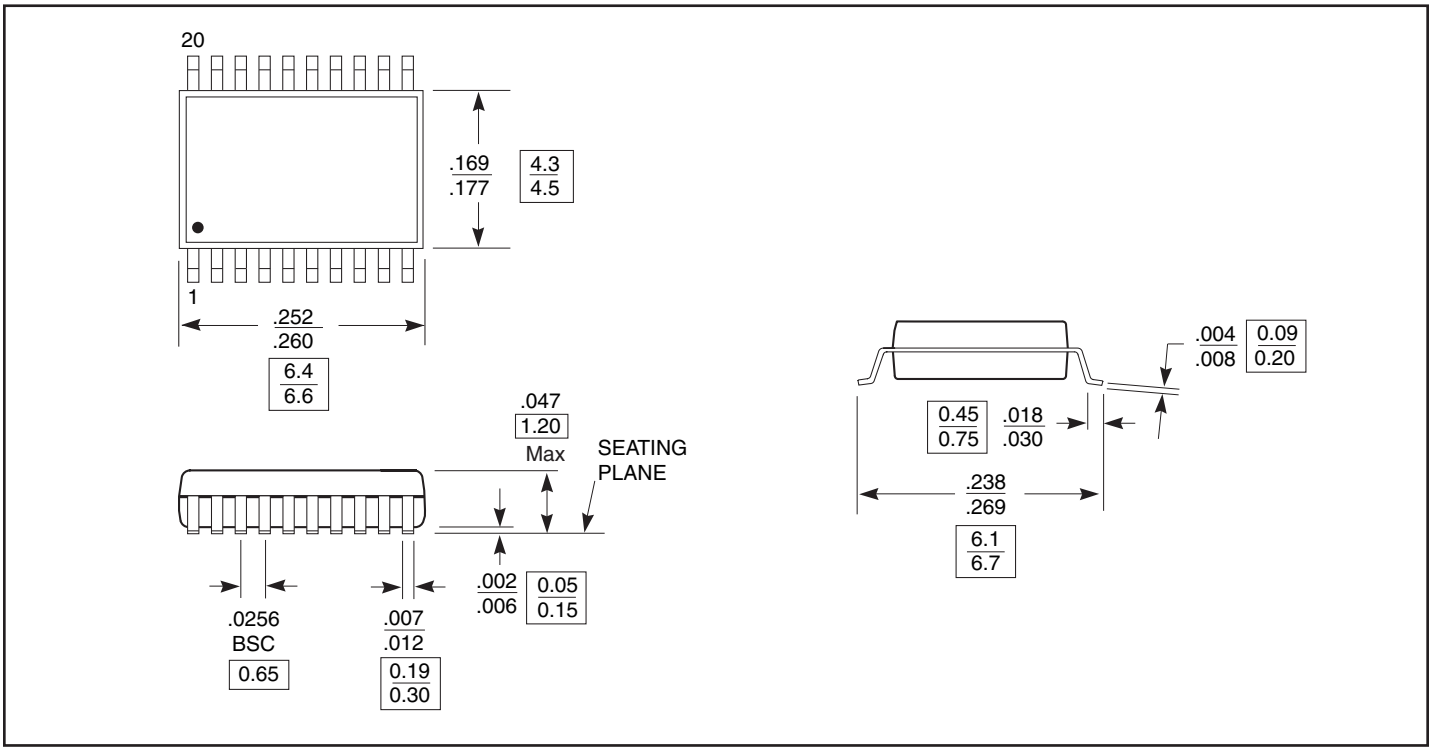
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
f_{max}	Output Frequency				500	MHz
t_{Pd}	Propagation Delay			1.5		ns
$T_{sk(o)}$	Output-to-output Skew			40		ps
t_r/t_f	Output Rise/Fall time	20% - 80%		150		
odc	Output Duty Cycle		48		52	%
J_{add}	Additive Jitter			30		fs

Notes:
1. All parameters are measured with CMOS input of 266MHz unless stated otherwise

Configuration Test Load Board Termination for LVPECL



Packaging Mechanical: 20-Pin TSSOP (L)



Ordering Information

Ordering Code	Package Code	Package Description
PI6C48535-01BLIE	L	Pb-free & Green 20-pin 173-mil wide TSSOP

Notes:

- Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
- E = Pb-free & Green
- X suffix = Tape/Reel